High Speed PCB & Spiral with Patch EBG Planar Integration for EMI Reduction

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***Abstract*—The need of high-speed printed circuit board design has increased in modern integrated circuitry while maintaining signal integrity and EMC standards as they became challenging issue. In this work, a high-speed PCB design which emitted high radiated emissions exceeding the EMC standard limits up to 4.54 GHz, has been fabricated and gone under radiated emission test. The EMI of the proposed PCB at 4.54 GHz has been suppressed using EBG spiral with patch planar that was integrated into the noisy PCB. Analyses of these characteristics indicate that the proposed EBG structures design is appropriate for the target EMI reduction.**

Keywords-Electromagnetic Interference(EMI); Electromagnetic Bandgap(EBG); Electromagnetic Compatibility(EMC); Radiated Emission (RE); Signal Integrity(SI); Printed Circuit Board (PCB)

I. Introduction

The speed of operation of printed circuit boards have increased as well as the data rate, and they become rapidly complex. They have led to the increased density of the circuits [1]. The variables in the lower frequency or higher rise time signals become more significant rather than being neglected with this increase. Electromagnetic emission from such circuitry is the contribution of high edge rate digital components along with the need for low power consumption. For this reasons, high-speed PCBs require extra care and alternative methods controlling the EMI introduced. EMI can be reduced by considering several strategies. These strategies may include, but are not limited to isolation of critical components, structure shielding, circuit grounding, impedance matching, signal filtering, involving of lossy materials or absorbers, and finally the possibility of circuitry redesign for victim device or the source of EMI. Eliminating the source of EMI is clearly desirable, but does not necessarily translate or equate to a reduction in the susceptibility of the device to external sources. In fact, substantial interference can occur at frequencies different from the frequencies corresponding to the device switching speed, which makes the containment strategies even more challenging [2].

In this work, EBG structure will be used to control EMI level on high-speed PCB that produce high radiated emission. They have sufficient characteristics for electromagnetic interference suppression with defined frequency range [3].

II. Spiral with Patch EBG Configuration

A. Mathematical Model

The resonance frequency of the L–C lumped elements has to be defined according to the target bandgap by using Eqn. 1. For this application of high radiated emissions proposed by high generating EMI printed circuit board, the target resonance was at 4 GHz. Therefore, the calculation of the values of L & C was achieved for the target resonance frequency. As shown in Eqn. 2, the L–C ratio has to be relatively high in order to obtain a wider stopband. As the inductance, L and capacitance, C values were known; the dimensions of the unit cell of the EBG structure were calculated using Greenhouse formulas based on lumped element model [4, 5].

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

While the relative bandwidth is proportional to:

$$\Delta BW \, \alpha \sqrt{\frac{L}{C}} \quad (2)$$

B. Greenhouse Formulas of Lumped Element Model

A self (L) and mutual (M_i) inductance of an inductor between the metallic sections (L_i) will provide expressions of the spiral geometries that were shown in Figure 1. The proposed geometries are represented by using Eqns. (3)-(5).

$$L\,(nH) = 2x10^{-4} L_i \,[\ln\left(\frac{L_i}{m+t}\right) + 1.193 + \frac{m+t}{3L_i}]\,.\,K \quad (3)$$

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$$Mi = 2x10^{-4}Li\ [\ln\{\frac{Li}{d}+\sqrt{(1+\frac{Li^2}{d^2})}\}-\sqrt{(1+\frac{d^2}{Li^2})}+\frac{d}{Li}]\quad (4)$$

$$C\ (pF) = 16.67x\ 10^{-4}Li\ \frac{\sqrt{\varepsilon r}}{Zo}\quad (5)$$

Where;

- L: Self inductance
- Mi: Mutual inductance of Section i
- C: Capacitance of the spiral with Patch Unit Cell
- Z_o: Surface impedance
- Li: Metallic Section
- ε_r: Dielectric constant
- K: Spacing constant
- m: Metallic width
- t: Metallic Thickness
- d: Distance between Middle Sections

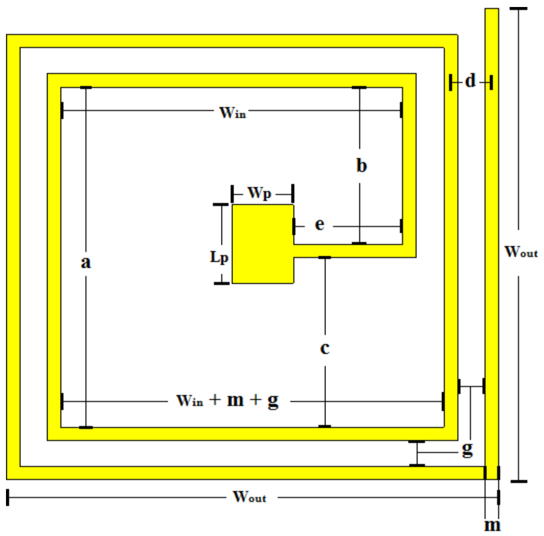

Figure 1. Metallic Sections of spiral withPatch EBG Unit Cell

The values of the geometrical parameters were shown in Table 1 in which they were calculated based on total inductance &capacitance respectively.

TABLE I. GEOMETRICAL PARAMETERS

Parameter		Value (mm)	Description
W_{out}		10.80	Metallic Outer Width
W_{in}		7.50	Internal Gaps of Unit Cell
a		7.80	
b		3.60	
c		3.90	
e		2.40	
g		0.60	Gaps Width
m		0.03	Metallic Width
d		0.09	Distance Between Middle Sections
Patch	*Wp*	1.35	Patch Width
	Lp	1.80	Patch Length

C. EBG Characteristic

The EBG unit cell was designed on a low-cost FR4 substrate with permittivity of 4.3 and thickness of 1.6mm. To verify the characteristic of the EBG, the waveguide model of the unit cell was simulated using CST Microwave Studio. The model of the waveguide defined two types of boundary conditions into two parallel walls with a wave port illuminated the surface from the top as depicted in Figure 2. In this simulation, the propagating plane wave was polarized parallel to the PMC walls and normal to the PEC walls.

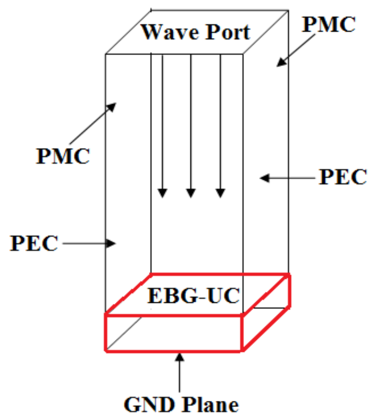

Figure 2. Waveguide Model

The simulation result of the reflection phase versus frequency for the EBG structure was depicted in Figure 3. It was clearly found that the proposed EBG is located at 4.08 GHz, having a narrow bandwidth of 70 MHz (4.05 – 4.12 GHz) within $90^0 \pm 45^0$ phase value.

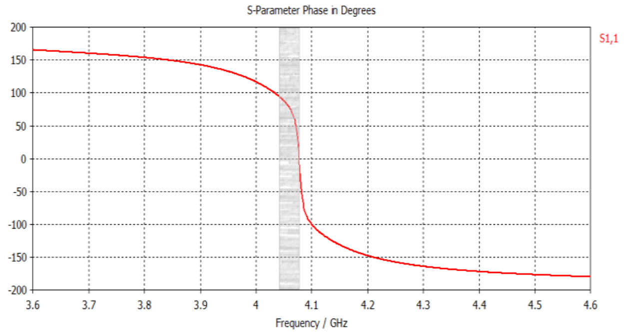

Figure 3. Reflection Phase of Spiral with Patch Unit Cell EBG

In addition, the characteristic of a 3 x 3 EBG structure is been analyzed and investigated using the suspended method [6]. A 50Ω suspended line was connected to two excitation ports at the ends of the line as shown in Figure 4. The simulated and measured characteristic results were illustrated in Figure 5. It was observed that, the EBG experienced bandgap from 4.5 GHz to 5.6 GHz for simulations and was extended in the measurements to 7 GHz with relative bandwidth of 43% that covers C band.

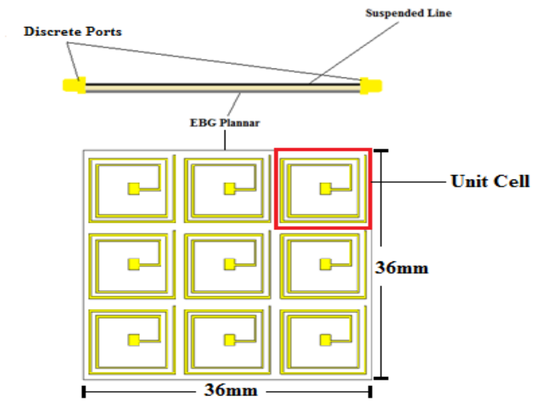

Figure 4. Suspended Microstrip Transmission Line Method

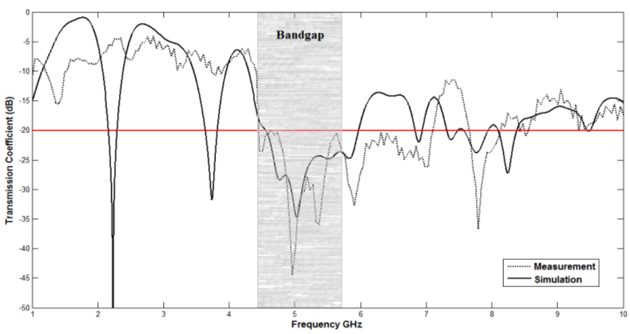

Figure 5. Transmission Coefficient S_{21} of 3 by 3 Spiral with Patch EBG planar.

It is worth to be noted that the resonances of the reflection phase in Figure 3 and suspended line transmission coefficient S_{21} in Figure 5 were apart from each other as shown previously. The reason of this differentiation was the contrasting computation schemes, and they were concerned with two different properties [7].

III. HIGH SPEED PRINTED CIRCUIT BOARD

In this section, radiated emission test for the high EMI printed circuit board has been experienced. The outcome of this testing was to verify that the RE of the source of EMI exceeded the limits above 4GHz. The mechanism of generating the radiated emissions was to break the EMC design guidance in order to obtain the required noise for EBG testing. In the development of high-speed printed circuit board, the following features had been considered [8]:

- Signal traces behave as transmission lines with a maximum length consideration.
- High operating frequency signals usually greater than 0.1 GHz.
- Small rise/fall time which is usually 1~2 ns range.

A. *Mathematical Analysis*

The definition of high-speed PCB involves the following parameters: trace impedance, propagation delay, trace length and the rise /fall time. These parameters were calculated using high-speed mathematical equations considered for the high-speed PCB design as shown in Eqns.(6)-(9).

$$Z_o=\left(\frac{79}{\sqrt{\varepsilon r+1.41}}\right).\ln\left(\frac{5.98H}{0.8W+T}\right)(\Omega) \quad (6)$$

$$T_{pd} = 1.017\sqrt{(0.475\varepsilon r) + 0.67} \quad (ns/ft) \quad (7)$$

$$L_{max} = 9\, t_r \ (cm) \quad (8)$$

$$T_r = 0.35/BW = \left(\frac{1}{10f}\right) \ (s) \quad (9)$$

Where;

- Z_o: Surface Impedance (Ω)
- H: Substrate Thickness (cm)
- T: Trace Thickness (cm)
- W:Trace Width (cm)

- T_{pd}: Propagation Delay (s)
- ε_r: Dielectric Constant
- L_{max}: Maximum Length (cm)
- T_r: Rise Time (s)
- BW: Bandwidth
- f: Operating Frequency (Hz)

B. High Radiated Emissions PCB Development

According to the EMC Guidance, the maximum length of the signal trace for the development of high-speed printed circuit board that was producing high RE above 4.5 GHz was 150 mm. However, in this work, the length of the traces was set to be 180 mm. This violation was for the purpose of verifying the EBG planar performance on the high-speed design circuit. For that reason, the proposed PCB shown in Figure 6 has the following design EMC guidance violations:

- Signal trace was electrically long with a length of 180mm with 90° angle corners, while the components and traces connected to the GND plane using vias.
- Increased the parasitic capacitance by increasing the operating frequency by using passive components such as R_L.
- By joining the high frequency & analog ground together
- Increased the separation between routing layer and GND plane; having a 3.2mm substrate thickness (T).

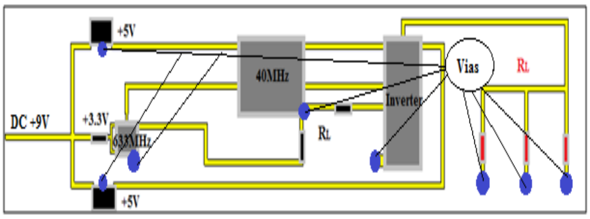

Figure 6. High Speed PCB Layout

C. Radiated Emission Test Results for HSPCB

The RE test was performed in semi anechoic chamber (SAC) in Electromagnetic Compatibility Lab, Universiti Tun Hussein Onn Malaysia (UTHM). The proposed PCB design shown in Figure 6 has high RE that reached 62dBuV/m exceeding EMC reading limit at 4.56 GHz as shown in Figure 7. Similarly, the RE also exceeded 70dBuV/m at 1.95 GHz. The increased number of pulses that defined the RE with respect to their corresponding frequency was four as can be seen. As the RE appeared above the 4 GHz exceeding the limit, this design was considered fulfill the requirement of our needs. Hence, the integration of spiral with patch EBG planar with the PCB will be investigated.

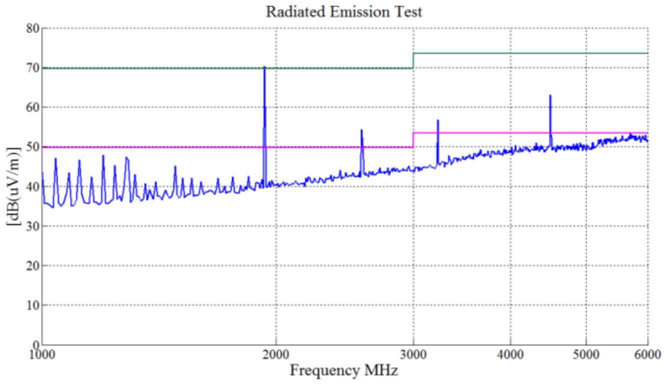

Figure 7. RE Test of High-Speed PCB at SAC

IV. SPIRAL WITH PATCH EBG PLANAR & PCB INTEGRATION

The integration of 15 x 3 EBG planar into a high-speed PCB which was producing high EMI brought good results as illustrated in Figure 8. As can be seen, the RE reduction was evident where the pulse that occurred at 4.5 GHz (as in Figure 7), was eliminated as shown in Figure 9. The EBG acted as a filter and suppressed the radiation that occurred at 4.5 GHz. The RE that appeared at 2, 2.6 and 3.3 GHz represented by pulses were not reduced as these frequencies are out of the EBG frequency bandgap.

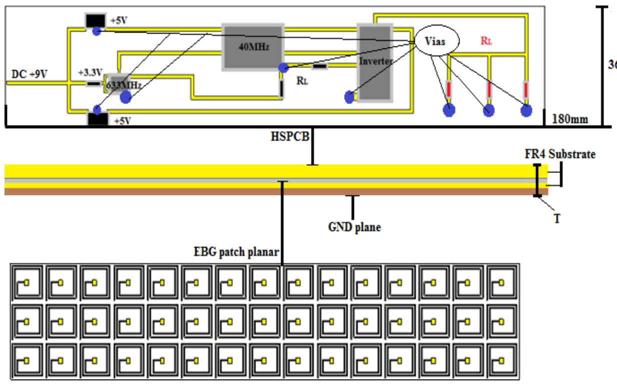

Figure 8. High-speed PCB and EBG planar Integration Layout

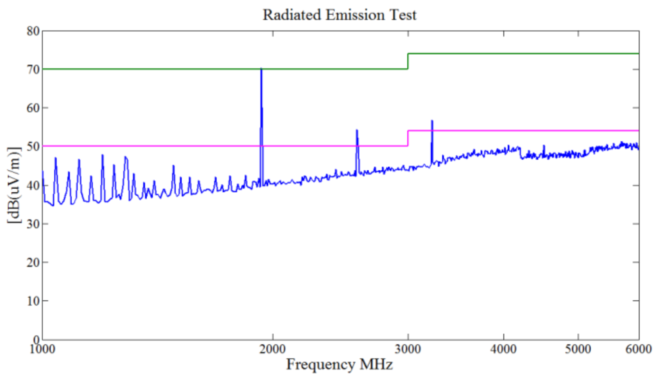

Figure 9. RE Test of High-speed PCB and EBG planar Integration

V. CONCLUSION

A 15x3 spiral with patch electromagnetic bandgap structure was simulated, measured and integrated into high source of EMI PCB design that violates the EMC design guidance for planar EBG testing. This integration has sufficient characteristics for suppressing the electromagnetic interference produced by PCB design with its violation within defined frequency range limited by the bandgap of the planar. It was obvious that the rest of pulses that occurred during the RE measurement for the integration have not been eliminated or suppressed as they were out of the planar bandgap range. Due to the complexity of PCB that increased with high speed of operation, data rate, and SI issues, EMI produced by such circuitries can be eliminated by using customized EBG planar according to their RE measurements that define the noise frequency spectrum. The spiral with patch EBG planar has proven good suppression within the design bandgap.

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REFERENCES

[1] Mark I. Printed Circuit Board Design Techniques for EMC Compliance.Second Edition. New York: John Wiley & Sons. 2000:99.

[2] Zhang W. The Electromagnetic Interference Model Analysis of the Power Switching Devices. *TELKOMNIKA Indonesian Journal of Electrical Engineering. 2013*; 11(1): 167-172.

[3] V. Adsure, H. Kroger and S. Weimin. Improving signal integrity in circuit boards by incorporating embedded edge terminations. *IEEE Transactions onAdvanced Packagin*g vol. 25, No.1, pp. 12-17 , Feb. 2002.

[4] M. A. Alshargabi, Z. Z. Abidin, M. Z. M. Jenu. Spiral Electromagnetic Bandgap structure for EMI reduction. *RF and Microwave Conference (RFM,2013)*310 - 313

[5] Bahl, I. Lumped Element for RF and Microwave Circuits.Norwood: Artech House.2003:34-36

[6] Kamal. A., Osman A., Thelaha M., Nazri A., Huda A. Electromagnetic Band Gap (EBG) StructureIn MicrowaveDevice Design. Unpublished Research Votes. *University Technology Malaysia*. No: 79017, pg.33, 2008.

[7] Islam M, Alam M. Compact EBG Structure for Alleviating Mutual Coupling between Patch Antenna Array Elements. *Progress In Electromagnetics Research.* Vol. 137, 425-483, 2013.

[8] Chai, C. C., Chung, B.K., Chuah, H. T.Simple Time Domain Expressions for Prediction of Crosstalk on Coupled Microstrip Lines. *Progress In Electromagnetics Research.* PIER39, 147-175, 2003.