2012 IEEE 7th International Power Electronics and Motion Control Conference - ECCE Asia
June 2-5, 2012, Harbin, China

Double-Switch Single-Inductor Resonant Cell Equalizer Using Voltage Multiplier for Series-Connected Supercapacitors

Masatoshi Uno and Akio Kukita
Institute of Space and Astronautical Science
Japan Aerospace Exploration Agency
3-1-1 Yoshinodai, Sagamihara, Kanagawa, Japan
uno.masatoshi@jaxa.jp

***Abstract*—Cell equalizers are usually used for series-connected energy storage cells, such as lithium-ion cells and supercapacitors (SCs), to eliminate voltage imbalance that may cause premature deterioration and reduce the available energies of the cells. Because conventional cell equalizers are based on multiple individual bidirectional dc-dc converters, the number of switches, inductors, and transformers increases proportionally with the number of series-connected energy storage cells. As compared to conventional equalizers, a double-switch resonant cell equalizer using a voltage multiplier, which is proposed in this paper, can reduce the circuit complexity significantly because of its double-switch single-inductor configuration. Furthermore, operation at a fixed frequency is feasible, and hence, feedback control can be eliminated. The fundamental operation is described in this paper. An experimental equalization test was performed for six series-connected SCs to demonstrate the equalization performance. The standard deviation of cell voltages decreased to approximately 5 mV at the end of the equalization process, thus verifying the proposed equalizer's performance.**

Keywords-equalizer; resonant inverter; supercapacitor (SC); voltage multipler; voltage imbalance

I. INTRODUCTION

Supercapacitors (SCs), including lithium-ion capacitors, which are hybrid capacitors combining features of conventional SCs and lithium-ion batteries, are energy storage devices that are superior to lithium-ion batteries in terms of life performance, power capability, temperature tolerance, and energy efficiencies. SCs have been mainly used in vehicular applications and regenerative systems in industries, in which energy buffers with high-power capability are required to meet short-term large power demands. Although specific energies of SCs are rather lower when compared to those of secondary batteries, SCs also have a great potential of being an alternative to traditional secondary batteries once their superior life performance over wide temperature range is factored in [1], [2].

Cell voltage imbalances originating from nonuniform individual cell properties of series-connected energy storage cells may cause premature deterioration due to overcharging and over-discharging, and may also reduce the available energy of the cells. As the number of series connections of energy storage cells increases, the nonuniformity of the cells tends to increase; therefore, any concerns about the cell voltage imbalance become more serious.

Various types of cell equalizers have been proposed and demonstrated for series-connected energy storage cells [3]–[5]. Most nondissipative equalizers are based on multiple connections of traditional individual bidirectional dc-dc converters, such as buck-boost converters [6]–[10], switched capacitor converters [11]–[18], and flyback converters [19]–[21]. Therefore, they require numerous switches, inductors, and transformers in proportion to the number of series connections of energy storage cells. In other words, circuit complexity and the cost of conventional cell equalizers tend to increase, particularly when the number of series connections is large. Equalizers using multi-winding transformers can dramatically reduce the required number of switches [22]–[24], but the application of multi-winding transformers to a large number of series connections becomes difficult because of the technical difficulty of strict parameter matching among multiple secondary windings [3],[4]. In order to reduce the number of components and the size of the equalizers, cell equalizers using a single converter and selection switches have been proposed for applications in lithium-ion batteries [25]–[27]. However, these equalizers still require numerous bidirectional switches, each of which is formed by two MOSFETs connected back-to-back, gate drive circuits, and voltage sensors.

Single-switch cell voltage equalizers based on multi-stacked buck-boost converters have been proposed [28]. These equalizers offer reduced circuit complexity and good modularity compared with the abovementioned equalizers because of the single-switch operation without the need for a multi-winding transformer. However, since multiple inductors are necessary, the circuits are prone to be bulky and costly as the number of series connections increases.

A double-switch single-inductor resonant cell equalizer using a voltage multiplier is proposed in this paper. Compared to conventional equalizers, the double-switch operation of the proposed equalizer can reduce the circuit complexity significantly. In addition, the equalization process in the

978-1-4577-2088-8/11/$26.00 ©2012 IEEE

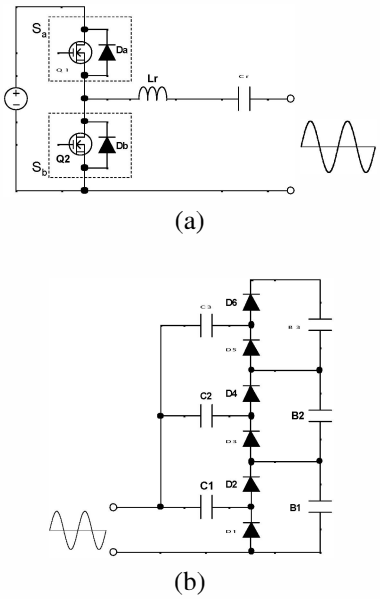


Figure 1. (a) Series resonant inverter and (b) voltage multiplier.

proposed equalizer proceeds automatically, enabling the control circuit to be simplified. The fundamental operation principle is described and a dc equivalent circuit is mathematically derived. An experimental equalization test for six SCs connected in series was performed to demonstrate and verify the equalization performance of the proposed equalizer.

II. Double-Switch Single-Inductor Resonant Equalizer using Voltage Multiplier

The proposed equalizer can be derived from the combination of a conventional series-resonant inverter shown in Fig. 1(a) and a voltage multiplier shown in Fig. 1(b), which is an example circuit that produces a voltage three times higher than the voltage amplitude of the input. In steady-state, each voltage across B_1–B_3 in the multiplier has a uniform value, which is the same as the amplitude of the input. A detailed operation analysis is presented in the following section.

The proposed double-switch single-inductor series-resonant equalizer for six SCs connected in series is shown in Fig. 2. Capacitors C_1–C_6, diodes D_1–D_{12}, and SCs SC_1–SC_6 compose a voltage multiplier, and C_1–C_6, all of which are tied to the resonant inductor L_r, together form a resonant capacitor, which corresponds to C_r in the conventional series-resonant inverter shown in Fig. 1(a). The input of the resonant equalizer is connected to the series connection of SC_1–SC_6. Therefore, the input power provided from the series connection of SC_1–SC_6 is redistributed to SC_1–SC_6 via the resonant cell equalizer. V_{ext} is an external voltage source, which represents an external charger in practical use.

In the proposed equalizer, only two switches are required, thus reducing the circuit complexity significantly when compared with conventional equalizers which require multiple switches in proportion to the number of series connections. In addition, the proposed equalizer can operate without any feedback control, and hence, the control circuit can be

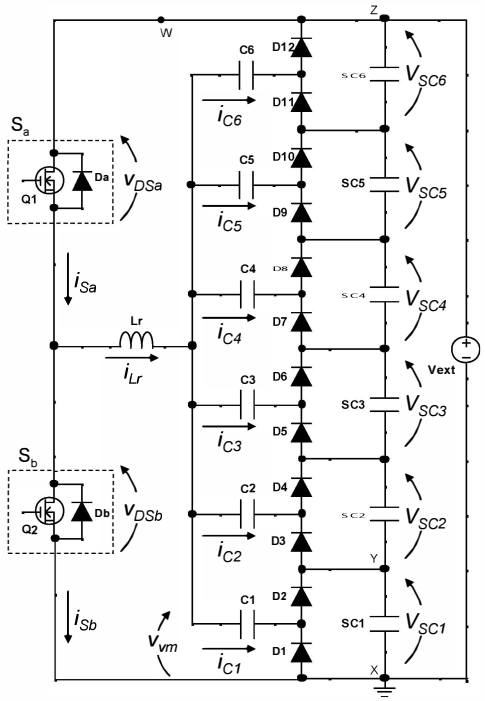


Figure 2. Double-switch single-inductor resonant equalizer using voltage multiplier for six SCs connected in series.

eliminated, further reducing the circuit complexity. We present an operation analysis, including waveform analysis and derivation of a dc equivalent circuit, in the following section.

The number of magnetic components can also be reduced. Conventional equalizers need a multi-winding transformer [21]–[24], multiple transformers [19],[20], or multiple inductors [6]–[10], [28] proportional to the number of series connections. On the other hand, the required magnetic component in the proposed equalizer is only one (L_r), and hence, the size and cost of the circuit are expected to be less than those of conventional equalizers.

III. Operation Analysis

A. Voltage Multiplier

Similar to conventional resonant inverters, the proposed resonant cell equalizer is operated at a switching frequency f higher than the resonant frequency. The resonant frequency under a voltage-balanced condition, f_r, is expressed as

$$f_r = \frac{1}{2\pi\sqrt{L_r\left(C_1 + C_2 + C_3 + C_4 + C_5 + C_6\right)}} \quad (1)$$

where L_r is the inductance of L_r, and C_1–C_6 are the capacitance of C_1–C_6. Under voltage-imbalanced conditions, f_r tends to be higher because some capacitors do not contribute to operations. An example of current flow paths under a voltage-imbalanced condition will be introduced in Section III C.

Theoretical key waveforms for $f > f_r$ are shown in Fig. 3. Two MOSFETs, Q_a and Q_b, alternately switch on and off with a fixed duty cycle of slightly less than 50% in order to provide

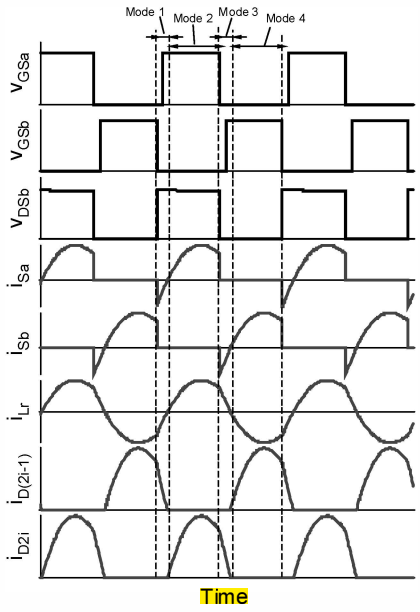


Figure 3. Key operation waveforms.

dead time. For $f > f_r$, the resonant circuit has an inductive characteristic, and the current through the resonant circuit, i_{Lr}, lags behind the fundamental component of the voltage v_{DSb}. Therefore, the switch currents, i_{Sa} and i_{Sb}, are negative right after switch-on, and are positive right before switch-off. Q_1 and Q_2 are switched-on at zero voltage for $f > f_r$, thus achieving zero voltage switching (ZVS) operations.

The operation of the equalizer can be divided into four modes: Mode 1–4. Current flow directions under a voltage-balanced condition in each mode are illustrated in Fig. 4. During Mode 1, the anti-parallel diode of Q_a, D_a, and odd-numbered diodes in the voltage multiplier are on. Negative switch currents in Fig. 3 represent current flowing through the anti-parallel diodes. SCs are charged by L_r and C_1–C_6 via the odd-numbered diodes. Before the current of S_a, i_{Sa}, reaches zero, the gate signal for Q_a (v_{GSa}) is applied. When i_{Sa} exceeds zero, Q_a turns-on at zero voltage and starts to conduct, and Mode 2 begins. SCs discharge to L_r and C_1–C_6 via the even-numbered diodes. As Q_a is switched-off, the current is diverted from Q_a to D_b, and the operation shifts to Mode 3. SCs are charged by L_r and C_1–C_6 via the even-numbered diodes. Before i_{Sb} becomes zero, the gate signal for Q_b (v_{GSb}) is applied. Mode 4 begins as i_{Sb} reaches zero and Q_b turns-on at zero voltage, and SCs start to discharge to L_r and C_1–C_6 via the odd-numbered diodes. As Q_b is turned-off, the current is diverted from Q_b to D_a, and the operation returns to Mode 1.

The voltages across C_1–C_6, V_{C1E}–V_{C6E}, when the even-numbered diodes are switched-on, can be expressed as

$$\begin{cases} V_{C1E} = -V_{VM-E} + V_D + V_{SC1} \\ V_{C2E} = -V_{VM-E} + V_D + V_{SC1} + V_{SC2} \\ V_{C3E} = -V_{VM-E} + V_D + V_{SC1} + V_{SC2} + V_{SC3} \\ V_{C4E} = -V_{VM-E} + V_D + V_{SC1} + V_{SC2} + V_{SC3} + V_{SC4} \\ V_{C5E} = -V_{VM-E} + V_D + V_{SC1} + V_{SC2} + V_{SC3} + V_{SC4} + V_{SC5} \\ V_{C6E} = -V_{VM-E} + V_D + V_{SC1} + V_{SC2} + V_{SC3} + V_{SC4} + V_{SC5} + V_{SC6} \end{cases} \quad (2)$$

where V_{VM-E} is the peak voltage across the voltage multiplier's input (as shown in Fig. 2) when the even-numbered diodes are on, and V_D is the forward voltage drop of the diodes. Similarly, the voltages across C_1–C_6, V_{C1O}–V_{C6O},when the odd-numbered diodes are on are

$$\begin{cases} V_{C1●} = V_{VM-●} - V_D \\ V_{C2●} = V_{VM-●} - V_D + V_{SC1} \\ V_{C3●} = V_{VM-●} - V_D + V_{SC1} + V_{SC2} \\ V_{C4●} = V_{VM-●} - V_D + V_{SC1} + V_{SC2} + V_{SC3} \\ V_{C5●} = V_{VM-●} - V_D + V_{SC1} + V_{SC2} + V_{SC3} + V_{SC4} \\ V_{C6●} = V_{VM-●} - V_D + V_{SC1} + V_{SC2} + V_{SC3} + V_{SC4} + V_{SC5} \end{cases} \quad (3)$$

where V_{VM-O} is the bottom voltage across the voltage multiplier's input when the odd-numbered diodes are on.

B. Derivation of DC Equivalent Circuit for Voltage Multiplier

The voltage variations across C_1–C_6 during a single switching cycle, ΔV_{C1}–ΔV_{C6}, can be obtained by subtracting (2) from (3):

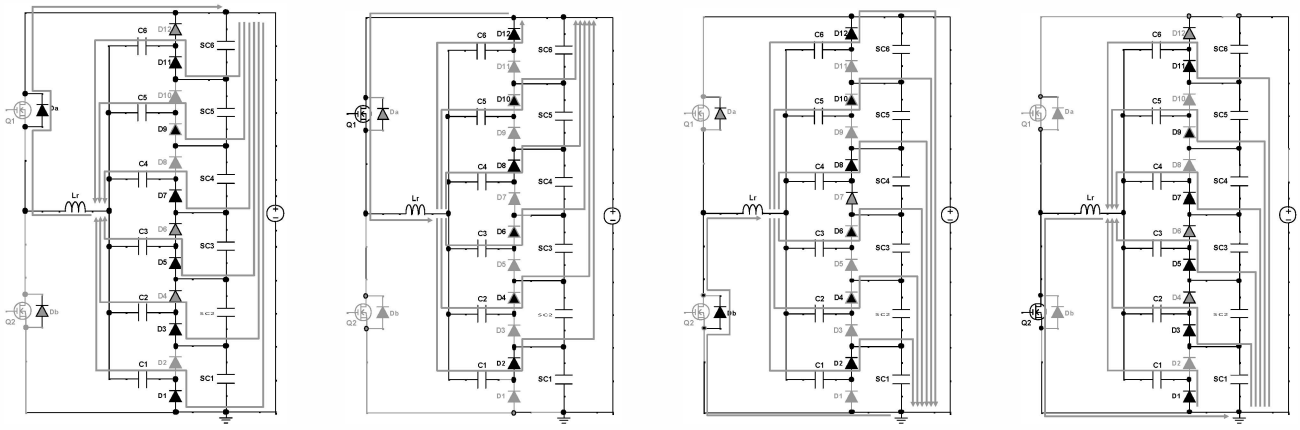


Figure 4. Current flow directions during Mode (a) 1, (b) 2, (c) 3, and (d) 4 under a voltage-balanced condition.

$$\begin{cases} \Delta V_{C1} = \left(V_{VM-E} + V_{VM-O}\right) - 2V_D - V_{SC1} \\ \Delta V_{C2} = \left(V_{VM-E} + V_{VM-O}\right) - 2V_D - V_{SC2} \\ \Delta V_{C3} = \left(V_{VM-E} + V_{VM-O}\right) - 2V_D - V_{SC3} \\ \Delta V_{C4} = \left(V_{VM-E} + V_{VM-O}\right) - 2V_D - V_{SC4} \\ \Delta V_{C5} = \left(V_{VM-E} + V_{VM-O}\right) - 2V_D - V_{SC5} \\ \Delta V_{C6} = \left(V_{VM-E} + V_{VM-O}\right) - 2V_D - V_{SC6} \end{cases} \quad (4)$$

In general, the amount of charge delivered via a capacitor and an equivalent resistance for the charge transfer are expressed as:

$$\begin{cases} Q = It = CV \\ V = \dfrac{It}{C} = \dfrac{I}{Cf} = IR_{eq} \end{cases} \quad (5)$$

From (4) and (5), the average currents flowing via C_1–C_6, I_{C1}–I_{C6}, can be obtained as:

$$\begin{cases} I_{C1}R_{eq1} = \left(V_{VM-O} + V_{VM-E}\right) - 2V_D - V_{SC1} \\ I_{C2}R_{eq2} = \left(V_{VM-O} + V_{VM-E}\right) - 2V_D - V_{SC2} \\ I_{C3}R_{eq3} = \left(V_{VM-O} + V_{VM-E}\right) - 2V_D - V_{SC3} \\ I_{C4}R_{eq4} = \left(V_{VM-O} + V_{VM-E}\right) - 2V_D - V_{SC4} \\ I_{C5}R_{eq5} = \left(V_{VM-O} + V_{VM-E}\right) - 2V_D - V_{SC5} \\ I_{C6}R_{eq6} = \left(V_{VM-O} + V_{VM-E}\right) - 2V_D - V_{SC6} \end{cases} \quad (6)$$

Equation (6) derives a dc equivalent circuit for the voltage multiplier that is shown in Fig. 5. All SCs are connected to the voltage source having a voltage level of (V_{VM-O} + V_{VM-E}) via two diodes and one equivalent resistor. The dc equivalent circuit indicates that SCs with the lowest voltage are preferentially charged via the equivalent resistors because of the common voltage source. Finally, all SC voltages converge to (V_{VM-O} + V_{VM-E} − $2V_D$) when I_{C1}–I_{C6} decrease down to zero.

C. Current Flow under Voltage-Imbalanced Condition

The derived dc equivalent circuit of the voltage multiplier provides intuitive understanding of how currents flow under

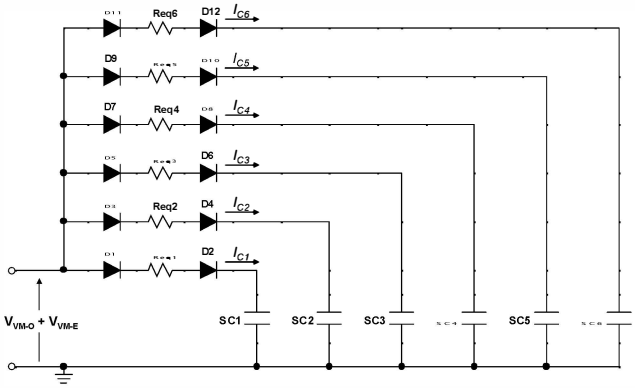


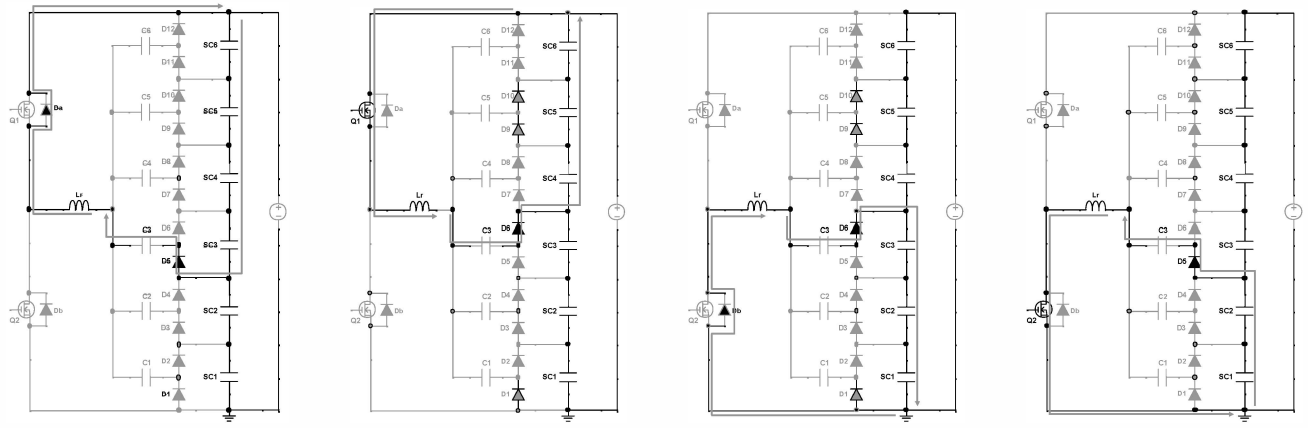
Figure 5. DC equivalent circuit of the voltage multiplier.

voltage-imbalanced conditions. For example, when V_{SC3} is the lowest among V_{SC1}–V_{SC6} (the dc equivalent circuit is shown in Fig. 5), the current preferentially flows through D_5, D_6, and R_{eq3} toward SC_3. This means that C_3 is the only capacitor that is charged and discharged during operations, as shown in Fig. 6, based on the analysis made in the previous subsection. Since all capacitors except C_3 do not contribute to operation, the resonant frequency f_r is determined by only L_r and C_3, and hence, f_r under voltage imbalance conditions is higher than that under a voltage-balanced condition. The current flow directions under other voltage-imbalanced cases can be explained in a similar manner.

D. Average Current Models for the Resonant Equalizer

In this subsection, the average current models for the resonant equalizer under a voltage-balanced condition are derived by assuming that the resonant equalizer operates at the resonant frequency f_r under a voltage-balanced condition.

From Figs. 4(b) and (c), the equivalent ac circuit of the proposed resonant equalizer can be derived as shown in Fig. 7. r_1–r_6 represent the ESR of each capacitor. The dc components in the voltage multiplier, i.e., V_{SC1}–V_{SC6} and V_D, are incorporated to the square wave generator designated as V_{ac}, which produces the square wave with the amplitude of (V_{in} − V_{SC} − $2V_D$). For voltage-imbalanced conditions, capacitors that do not contribute to the operations should be removed from the



(a) (b) (c) (d)

Figure 6. Current flow directions during Mode (a) 1, (b) 2, (c) 3, and (d) 4 under a voltage-imbalanced condition where V_{SC3} is the lowest among V_{SC1}–V_{SC6}.

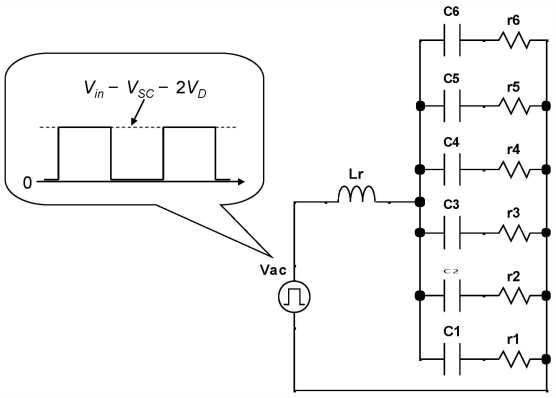


Figure 7. AC equivalent circuit of the proposed resonant cell equalizer under a voltage-balanced condition.

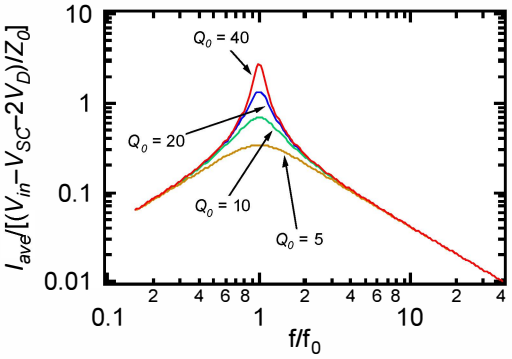


Figure 8. Normalized current of I_{ave} as a function of f/f_0.

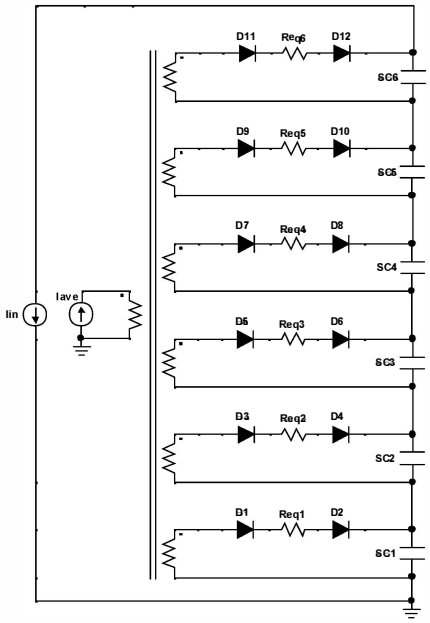


Figure 9. DC equivalent circuit of the resonant equalizer.

ac equivalent circuit. For example, when V_{SC3} is the lowest among V_{SC1}–V_{SC6}, only L_r, C_3 and r_3 form the ac equivalent circuit. Following analyses are focused on a voltage-balanced condition, although similar developments can be made for voltage-imbalanced conditions.

The voltage amplitude of the fundamental component of the square wave can be expressed using the Fourier transform as

$$V_m = \frac{2}{\pi}\left(V_{in} - V_{SC} - 2V_D\right) \tag{7}$$

where V_{in} is the sum of V_{SC1}–V_{SC6}.

The input impedance of the resonant equalizer is

$$\begin{aligned} |Z| &= \sqrt{r_{tot}^2 + \left(\omega L_r - \frac{1}{\omega C_{tot}}\right)^2} \\ &= Z_0\sqrt{\frac{1}{Q_0^2} + \left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2} \end{aligned} \tag{8}$$

where

$$\begin{cases} r_{tot} = r_1 \| r_2 \| r_3 \| r_4 \| r_5 \| r_6 \\ C_{tot} = C_1 + C_2 + C_3 + C_4 + C_5 + C_6 \\ Z_0 = \omega_r L = \dfrac{1}{\omega_r C_{tot}} \\ Q_0 = \dfrac{Z_0}{r_{tot}} \end{cases} \tag{9}$$

and Z_0 is the characteristic impedance of the resonant equalizer, and Q_0 is the unloaded quality factor.

Generally, the voltage conversion ratio of equalizers is fixed because both the input and output of equalizers are a voltage source. Therefore, the currents in the equalizers should be controlled or limited under the desired current levels in order to avoid excess currents, which may destroy the circuit. The amplitude of the current flowing through L_r is given by

$$I_m = \frac{V_m}{|Z|} \tag{10}$$

The average current of L_r in a half switching cycle, I_{ave}, is expressed as

$$\begin{aligned} I_{ave} &= \frac{I_m}{\pi}\int_0^{\pi} \sin(\omega t)\, d(\omega t) = \frac{2I_m}{\pi} \\ &= \left(\frac{2}{\pi}\right)^2 \frac{V_{in} - V_{SC} - 2V_D}{Z_0\sqrt{\frac{1}{Q_0^2} + \left(\frac{\omega}{\omega_r} - \frac{\omega_r}{\omega}\right)^2}} \end{aligned} \tag{11}$$

The input current for the equalizer, I_{in}, is equal to that of S_a, and hence,

$$I_{in} = \frac{I_{ave}}{2} \tag{12}$$

The normalized current of I_{ave} under a voltage-balanced condition is shown in Fig. 8. Equation (11) indicates that I_{ave} is proportional to $(V_{in} - V_{SC} - 2V_D)$, and tends to be quite large at ω_r (f_r) at which Z_0 becomes quite small because V_{in} is almost six times as high as V_{SC} in the example of the proposed equalizer shown in Fig. 2. Therefore, the switching frequency f should be determined rather higher than f_r so that currents can be limited under the desired levels by increasing $|Z|$, which is expressed by (8). An alternative way to limit currents is the use of a transformer to match V_{in} and V_{SC}, although it results in an increased size of the equalizer. With a fixed value of $|Z|$ and known variation ranges of V_{in} and V_{SC}, I_{in} and I_{ave} as well as capacitor currents, which are represented as I_{C1}–I_{C6}, can be limited under a desired current level. Hence no feedback control is necessary to limit the equalization currents in the proposed cell equalizer.

The dc equivalent circuit of the proposed resonant equalizer can be derived from (6), (11), and (12), as shown in Fig. 9. The equivalent circuit of the voltage multiplier shown in Fig. 5 is modified in Fig. 9; an ideal multi-winding transformer, with a turn ratio of 1:1 is used in order for SC_1–SC_6 to be connected in series. This equivalent circuit provides qualitative understanding of how the cell voltages are balanced by the proposed equalizer. The series connection of SC_1–SC_6 provides energies to the equalizer in the form of I_{in}, and the provided energies are redistributed via the voltage multiplier in the form of I_{ave}. I_{ave} is distributed to SC_1–SC_6 depending on their voltages. The voltages across SCs with higher voltages decrease by providing energies to the equalizer, while the voltages of SCs with lower voltages increase by receiving the energies from the voltage multiplier. All the SC voltages eventually become uniform as long as R_{eq} and V_D for each SC are uniform.

Table 1. Component values for the prototype.

Component	Value
C_1-C_6	Tantalum Capacitor, 10 µF
C_{in}	Tantalum Capacitor, 47 µF
C_{out1}-C_{out6}	Ceramic Capacitor, 200 µF
L_1	10 µH
Q_a,Q_b	N-Ch MOSFET, HAT2266H, R_{on} = 9.2 mΩ
D_1-D_{12}	Schottky Diode, CRS08, V_D = 0. 36 V

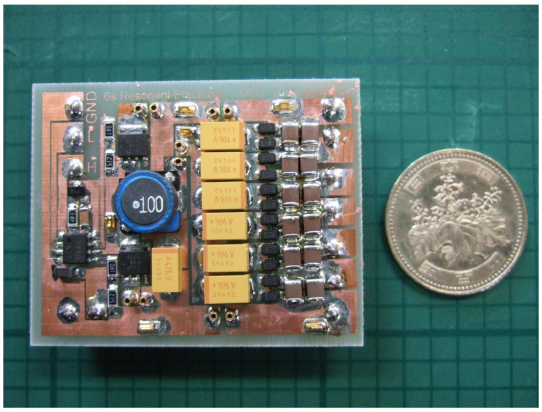


Figure 10. Photograph of a 2 W Prototype of the proposed double-switch single-inductor resonant cell equalizer.

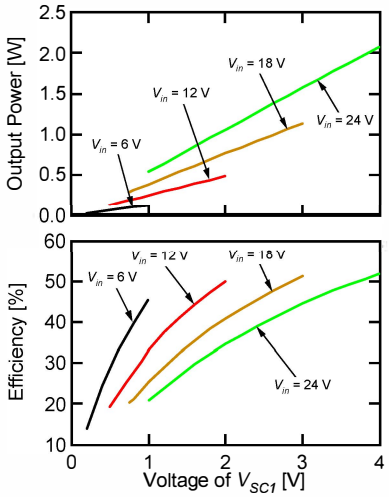
IV. Experiment

A. Prototype

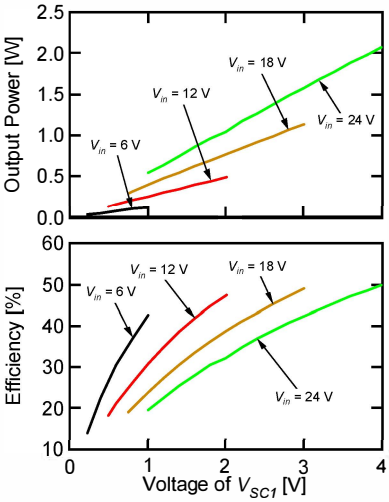
A 2 W prototype of the proposed resonant cell equalizer was designed for six series-connected SCs. Component values and a photograph of the prototype are shown in Table 1 and Fig. 10, respectively. C_{in} and C_{out1}–C_{out6} denote smoothing capacitors, which were connected in parallel to the input and SC_1–SC_6, respectively. The prototype was operated at a fixed switching frequency of 100 kHz with a fixed duty cycle of 45%.

B. Power Conversion Efficiencies under Voltage-Balanced and Voltage-Imbalanced Conditions

The power conversion efficiencies of the prototype were measured with emulating voltage-balanced and voltage-imbalanced conditions. The terminal W shown in Fig. 2 was broken in order to separate the input and output of the equalizer, and the input voltage was supplied to the half-bridge inverter



(a)



(b)

Figure 11. Power conversion efficiencies under (a) voltage-balanced and (b) voltage-imbalanced conditions.

while the variable resistor was connected between terminal X and Z, and X and Y for voltage-balanced and voltage-imbalanced conditions, respectively. The external voltage source V_{ext} was removed during the efficiency measurement. The supplied voltage V_{in} was 6, 12, 18, or 24 V, and the power conversion efficiencies were measured with changing the ratio of V_{SC1}/V_{in} between 1/24 and 1/6.

The measured power conversion efficiencies and output powers under voltage-balanced and voltage-imbalanced conditions are shown in Figs. 11(a) and (b), respectively. The efficiencies increased with V_{SC1}. This tendency indicates that losses in diodes represented a significant portion of the output powers, especially when V_{SC1} was relatively low. Measured efficiencies under the voltage-balanced conditions were slightly higher than those under the voltage-imbalanced conditions. These lower efficiencies can be attributed to the current concentration of SC_1 as well as C_1 that causes increased Joule loss in the ESR of C_1. This can be better explained by the dc equivalent circuit derived in Fig. 9; the current concentration under the voltage-imbalanced condition causes an increased Joule loss in R_{eq1}.

Measured waveforms of i_{Lr} and v_{DSb} at V_{in} = 18 V and V_{SC1} = 3.0 V under the voltage-balanced and voltage-imbalanced conditions are shown in Fig. 12. The waveforms were independent on whether voltages were balanced or imbalanced, and almost identical waveforms were observed. The waveforms of i_{Lr} were almost triangular because the switching frequency f was determined to be rather higher than f_r to limit currents, as discussed in Section III D. The triangular waves imply that circulation currents flowing through the anti-parallel diodes (D_a and D_b) are large and undermine the power conversion efficiencies. In addition, the larger the circulation currents, the larger will be the turn-off switching losses, further undermining the efficiencies. In order for i_{Lr} to be sinusoidal to reduce the circulation currents, a transformer should be incorporated into the resonant circuit to match V_{in} and V_{SC} so that f can be determined as close to f_r as possible, as discussed in Section III D.

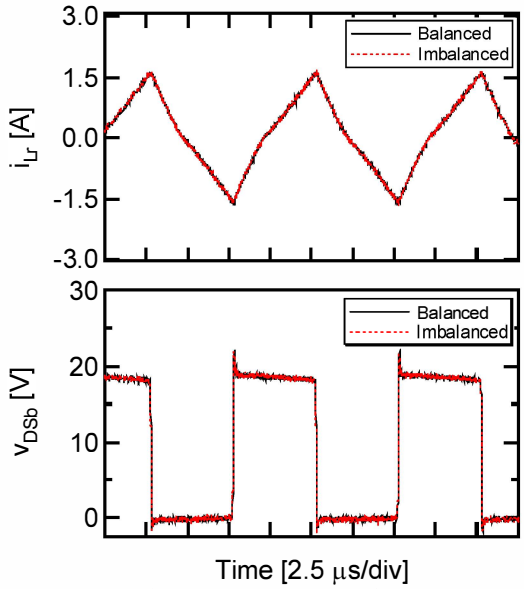


Figure 12. Measured operation waveforms under voltage-balanced and -imbalanced conditions.

C. *Equalization Test*

SCs with a capacitance of 500 F at a rated charge voltage of 2.5 V were used for the experimental equalization test. Six SCs, whose initial voltages were intentionally imbalanced as 1.0, 1.3, 1.6, 1.9, 2.2, and 2.5 V, were equalized by the prototype of the proposed equalizer. The voltage of V_{ext} was 10.5 V, which was the same as the total voltage of V_{SC1}–V_{SC6}. The resultant equalization profiles are shown in Fig. 13.

As explained in Section III, the energies of the series-connected SCs were preferentially redistributed to the SCs with the lowest voltage. In other words, SCs with the lowest voltage were charged by the equalizer, while others were discharged. The voltage imbalance was gradually eliminated as time elapsed, and all SC voltages converged to 1.75 V, which was the average of initial SC voltages, due to V_{ext} complementing energy losses in the equalizer during the equalization process. The standard deviation decreased down to approximately 5 mV at the end of the experiment, verifying the equalization performance of the proposed resonant cell equalizer.

V. Conclusions

A double-switch single-inductor resonant cell equalizer using a voltage multiplier was proposed in this paper. The double-switch operation without feedback control can reduce the circuit complexity significantly by reducing the number of required switches compared with conventional equalizers, and

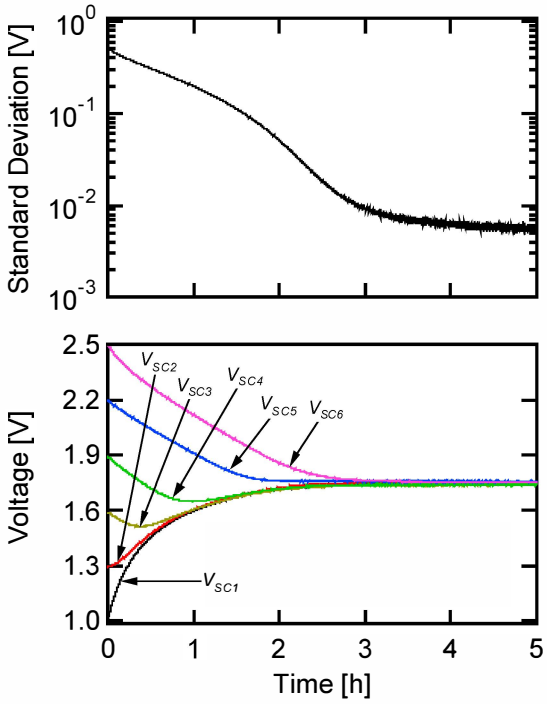


Figure 13. Experimental equalization profiles of six SCs connected in series.

eliminating feedback control. In addition, since the proposed equalizer operates with a single inductor, the equalizer can be designed with a small form-factor. Thus, the double-switch single-inductor circuit configuration provides a number of major advantages over conventional topologies.

The fundamental operation of the proposed equalizer was analyzed, and the dc equivalent circuit was derived based on the mathematical analysis to prove the voltage equalization mechanism.

An experimental equalization test using a 2 W prototype operating at a fixed frequency with a fixed duty cycle was performed for six SCs connected in series from an initially voltage-imbalanced condition. The cell voltage imbalance was gradually eliminated, and the standard deviation decreased down to approximately 5 mV at the end of the experiment.

Our future research focuses on the series-resonant equalizer with a transformer to improve power conversion efficiencies, and search for suitable topologies of resonant inverters for equalizers using a voltage multiplier.

REFERENCES

[1] M. Uno and K. Tanaka, "Accelerated charge-discharge cycling test and cycle life prediction model for supercapacitors in alternative battery applications," *IEEE Trans. Ind. Electron.*, to be published.

[2] M. Uno and K. Tanaka, "Spacecraft electrical power system using lithium-ion capacitors," *IEEE Trans. Aerosp. Electron. Syst.*, to be published.

[3] J. Cao, N. Schofield, and A. Emadi, "Battery balancing methods: a comprehensive review," in *Proc. IEEE Veh. Power and Propulsion Conf.*, pp. 1–6, Sep. 2008.

[4] K. Z. Guo, Z. C. Bo, L. R. Gui, and C. S. Kang, "Comparison and evaluation of charge equalization technique for series connected batteries," in *Proc. IEEE Power Electron. Spec. Conf.*, pp. 1–6, Jun. 2006.

[5] D. Linzen, S. Buller, E. Karden, and R. W. De Doncker, "Analysis and evaluation of charge-balancing circuits on performance, reliability, and lifetime of supercapacitor systems," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1135–1141, Sep./Oct. 2005.

[6] K. Nishijima, H. Sakamoto, and K. Harada, "A PWM controlled simple and high performance battery balancing system," in *Proc. IEEE Power Electron. Spec. Conf.*, pp. 517–520, Jun. 2000.

[7] Y. S. Lee, M. W. Cheng, S. C. Yang, and C. L. Hsu, "Individual cell equalization for series connected lithium-ion batteries," *IEICE Trans. Commun.*, vol. E89-B, no. 9, pp. 2596–2607, Sep. 2006.

[8] Y. S. Lee and M. W. Cheng, "Intelligent control battery equalization for series connected lithium-ion battery strings," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1297–1307, Oct. 2005.

[9] C. S. Moo, Y. C. Hsieh, and I. S. Tsai, "Charge equalization for series-connected batteries," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 39, no. 2, pp. 704–710, Apr. 2003.

[10] P. A. Cassani and S. S. Williamson, "Feasibility analysis of a novel cell equalizer topology for plug-in hybrid electric vehicle energy-storage systems," *IEEE Trans. Veh. Technol.*, vol. 58, no. 8, pp. 3938–3946, Oct. 2009.

[11] C. Pascual and P. T. Krein, "Switched capacitor system for automatic series battery equalization," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, pp. 848–854, Feb. 1997.

[12] J. W. Kimball, B. T. Kuhn, and P. T. Krein, "Increased performance of battery packs by active equalization," in *Proc. IEEE Veh. Power Propulsion Conf.*, pp. 323–327, Sep. 2007.

[13] A. Baughman and M. Ferdowsi, "Double-tiered switched-capacitor battery charge equalization technique," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 2277–2285, Jun. 2008.

[14] M. Uno and K. Tanaka, "Influence of high-frequency charge-discharge cycling induced by cell voltage equalizers on the life performance of lithium-ion cells," *IEEE Trans. Veh. Technol.*, Vol. 60, No. 4, pp. 1505–1515, May. 2011.

[15] R. Lu, C. Zhu, L. Tian, and Q. Wang, "Super-capacitor stacks management system with dynamic equalization techniques," *IEEE Trans. Magnetics*, vol. 43, no. 1, pp. 254–258, Jan. 2007.

[16] M. Uno and H. Toyota, "Supercapacitor-based energy storage system with voltage equalizers and selective taps," in *Proc. IEEE Power Electron. Spec. Conf.*, pp. 755–760, Jun. 2008.

[17] M. Uno and H. Toyota, "Equalization technique utilizing series-parallel connected supercapacitors for energy storage system," in *Proc. IEEE Int. Conf. Sustainable Energy*, pp. 999–1003, Nov. 2008.

[18] H. S. Park, C. H. Kim, K. B. Park, G. W. Moon, and J. H. Lee, "Design of a charge equalizer based on battery modularization," *IEEE Trans. Veh. Technol.*, vol. 58, pp. 3216–3223, Sep. 2009.

[19] H. S. Park, C. E. Kim, C. H. Kim, G. W. Moon, and J. H. Lee, "A modularized charge equalizer for an HEV lithium-ion battery string," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1464–1476, May 2009.

[20] C. H. Kim, H. S. Park, C. E. Kim, G. W. Moon, and J. H. Lee, "Individual charge equalization converter with parallel primary winding of transformer for series connected lithium-ion battery strings in an HEV," *J. Power Electron.*, vol. 9, no. 3, pp.472–480, May 2009.

[21] M. Y. Kim, C. H. Kim, S. Y. Cho, and G. W. Moon, "A cell selective charge equalizer using multi-output converter with auxiliary transformer," in *Proc. 8th Int. Conf. Power Electron. ECCE Asia*, pp. 310–317, Jun. 2011.

[22] N. H. Kutkut, D. M. Divan, and D. W. Novotny, "Charge equalization for series connected battery strings," *IEEE Trans. Ind. Appl.*, vol. 31, no. 3, pp. 562–568, May/Jun. 1995.

[23] N. H. Kutkut, H. L. N. Wiegman, D. M. Divan, and D. W. Novotny, "Charge equalization for an electrich vehicle battery system," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 34, no. 1, pp. 235–246, Jan. 1998.

[24] N. H. Kutkut, H. L. N. Wiegman, D. M. Divan, and D. W. Novotny, "Design considerations for charge equalization of an electric vehicle battery system," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 28–35, Jan. 1999.

[25] A. M. Imtiaz, F. H. Khan, and H. Kamath, "Steady state analytical model of a "time shared Li-ion cell balancing circuit" for plug-in hybrid vehicles and utility energy storage," in *Proc. 8th Int. Conf. Power Electron. ECCE Asia*, pp. 577–584, Jun. 2011.

[26] C. H. Kim, M. Y. Kim, Y. D. Kim, and G. W. Moon, "A modularized charge equalizer using battery monitoring IC for series connected Li-ion battery string in an electric vehicle," in *Proc. 8th Int. Conf. Power Electron. ECCE Asia*, pp. 304–309, Jun. 2011.

[27] M. Y. Kim, J. W. Kim, C. H. Kim, S. Y. Cho, and G. W. Moon, "Automatic charge equalization circuit based on regulated voltage source for series connected lithium-ion battery," in *Proc. 8th Int. Conf. Power Electron. ECCE Asia*, pp. 2248–2255, Jun. 2011.

[28] M. Uno and K. Tanaka, "Single-switch cell voltage equalizer using multistacked buk-boost converters operating in discontinuous conduction mode for series-connected energy storage cells," *IEEE Trans. Veh. Technol.*, Vol. 60, No. 8, pp. 3635–3645, Oct. 2011.