

# Area-efficient Low-Power 8-Bit 20-MS/s SAR ADC in 0.18µm CMOS

E. Atkin, D. Normanov

*Abstract* - This paper presents the design results of the prototype IP block of the successive approximation analog-to-digital converter (SAR ADC) for implementation by 0.18 µm MMRF CMOS technology of UMC (Taiwan).

Primarily the ADC unit was designed according to the technical requirements for the readout electronics of the silicon tracking system of the Compressed Baryonic Matter experiment at accelerator facility FAIR ([www.gsi.de/en/research/fair.htm](http://www.gsi.de/en/research/fair.htm)). However it can be used for a wider range of applications.

To increase accuracy and ensure ADC resolution a rail-to-rail comparator was used. The SAR ADC occupies on chip area of 325µm x 325µm, ENOB is 6.88 bits, maximum DNL less than 0.8 LSB, an INL less than 0.6 LSB, sampling frequency – 20 MHz, clock frequency – 200 MHz, and SNDR is 43.2 dB. With these parameters the ADC consumes about 1.3 mA at a nominal supply voltage of 1.8V.

## I. INTRODUCTION

At building application-specific integrated circuits (ASIC) for different systems of detector data readout one of the important blocks is the analog-to-digital converter (ADC). In particular, ADCs are required for the multichannel data-driven system for collecting and processing data with the function of analogue derandomization, designed [1], [2] for the CBM experiment at the international accelerator facility FAIR.

The main requirements to an ADC for this application are: small area occupied on chip, low power consumption and medium speed (10-100 MS/s). In order to satisfy the technical requirements for the readout electronics of the CBM silicon tracking system, the pipeline architecture and successive approximation ADC are used as the most popular solutions [3]. At comparing these two architectures, from a number of modern works [4-7], the analog-to-digital converter with successive approximation (SAR) looks preferable against the pipelined ADC for the medium range of sampling rates, because of the greater power consumption and larger on chip area [3].

In this paper we present the design of SAR ADC in the 0.18µm CMOS process, which uses the charge redistribution DAC, designed to achieve good accuracy, low power consumption and the small area on chip. Although more advanced technologies allow the ADC to get a better performance [3], the UMC 0.18 µm used by

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FAIR community as standard.

In order to meet the specifications for power consumption, the ADC uses a digital-to-analog converter (DAC) based on the algorithm of charge-redistribution instead of the DAC based on resistors [8]. It should be noted, that the DAC provides a charge-redistribution for a capacitor array, resulting in an increased accuracy and more chip area, compared to the circuit based on the resistor array. To reduce the area occupied by the on-chip ADC it was decided to make a single ended DAC with one capacitor. To ensure accuracy comparator is made with the rail-to-rail [9] function for input. Thanks to this ADC, proposed in this paper, achieves high resolution and accuracy with one input.

Founded on the above points, this paper presents a moderate sample speed SAR ADC, which employs a common-centroid symmetry layout, SAR reset circuit and rail-to-rail comparator. As result, the ADC has a low power, and occupies a small area of chip.

## II. ADC ARCHITECTURE

Fig. 1 shows a block diagram of the developed prototype of an 8-bit analog-to-digital converter, which contains a sample and hold circuit (SH), a DAC, a comparator and SAR control block.

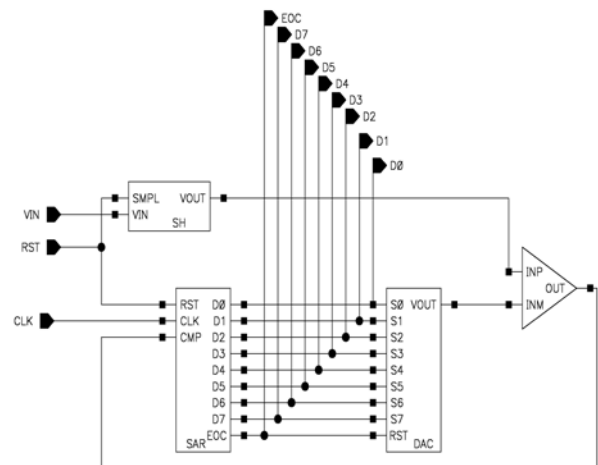


Figure 1: Block diagram of the SAR ADC

### A. ADC cycle

The operation cycle of the ADC can be divided into the following steps:

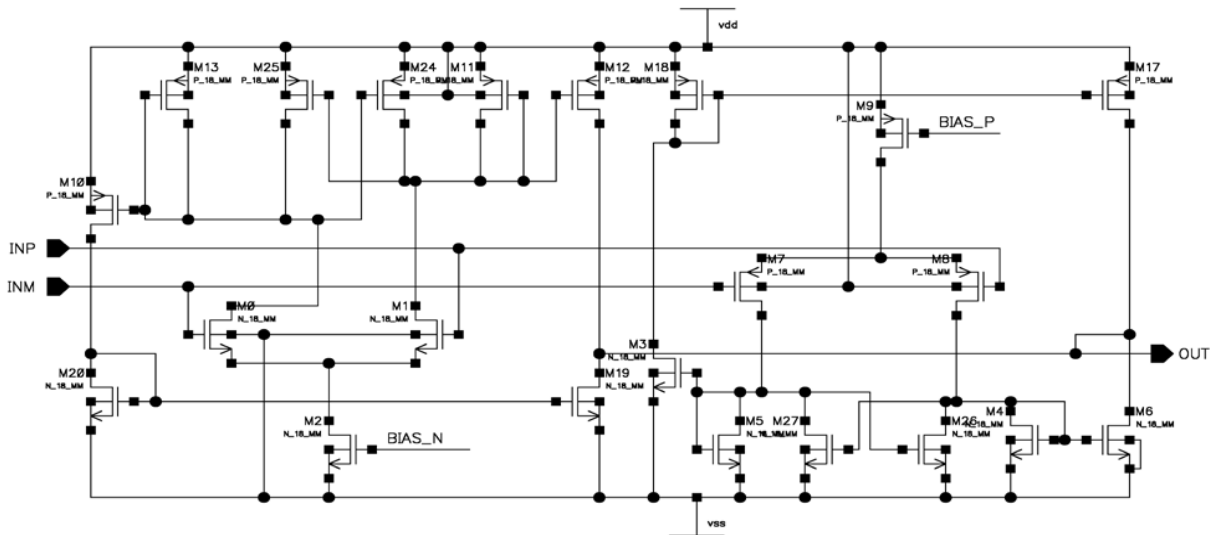


Figure 2: Comparator with the rail-to-rail function for Input

- on the arrival of the signal RST, there is reset the voltage of the successive approximation register and DAC.
- The SH enters the sampling phase and begins to record the current level of input charge.
- The successive-approximation-register turns on the DAC MSB, having the largest capacity of 128Cunit, the DAC forms a voltage, equal to a half the full transformation scale.
- The comparator decides if the MSB should remain high or set low during the conversion.
- Comparison continues until all the values of output bits are determined.
- After identifying all 8 bits, the signal of count finish EOC is generated, the ADC retains its value until the next reset signal RST.

**B. Comparator**

The comparator is shown in Fig. 2. It is necessary for an accurate comparison, of the input voltage level with the voltage, fixed by SHA coming from the DAC. It has the function of rail-to-rail for input to provide the required accuracy.

The circuits with two parallel complementary parts allow to cover the entire range of input voltages. Their

output signals are combined in a current summing circuit and converted into voltage. Loads for the differential input stages are the diode-connected and cross-coupled transistors, which lower the output impedance of the load of the first stage of the comparator, as well as increase its gain [10]. The current outputs of the first stage are fed to the diode (as a transistor) that converts a current signal into a voltage, and a second comparator stage: a common source.

The power supply of the comparator uses self-biasing reference with short-channel transistors [10].

The designed comparator at signal of 20 MHz consumes 300 uA at an average, its voltage gain is 65 dB at a unity gain frequency of 230 MHz, the maximum switching time is 3.75 ns.

**C. SAR logic**

Fig. 3 shows the successive approximation register, circuit, based on the serial shift register. It is acting as a mask for the current discharge comparison and storage recursive register, that stores the current result of the conversion. The synchronized by the front D-flip-flops with asynchronous reset and setting are the main element of the block [11].

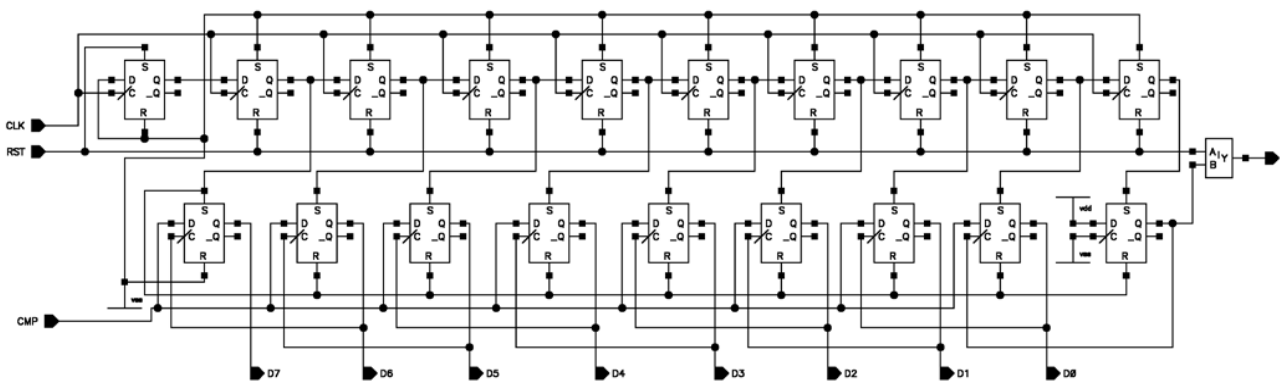


Figure 3: SAR logic

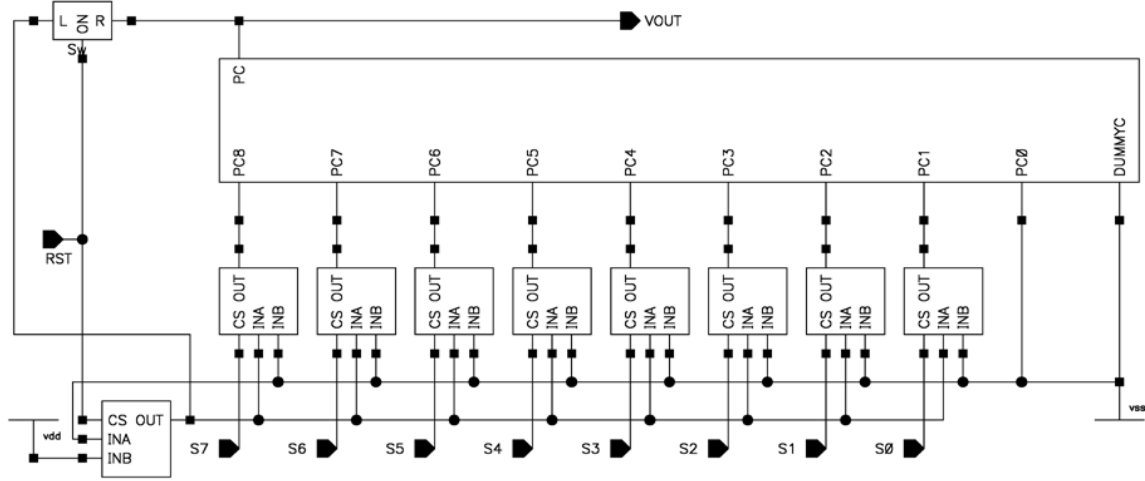


Figure 4: DAC Block diagram

Positive signal RST reset clears serial register by recording 1 into its of his first trigger and preventing clocking by storing the result of the previous conversion. Next after resetting logic 0 the clock resets an accumulating register and the mask changes its MSB to logical unit, EOC (end of conversion) goes to logic 0, inverting only after comparing the least significant bit.

#### D. DAC

The DAC of Fig. 4 is made with a binary-weighted array of capacitors with a reference capacitance  $C_{unit} = 10fF$ , since this solution provides the best linear transformation, and a number of key elements for switching the capacitors to ground or power supply.

An important task is to design the specialized topology array of capacitors in order to ensure maximum matching accuracy of array elements, and, as a consequence, the minimum deviation of the relative ratings of array elements.

One problem is that when manufacturing the mask, having bias influencing the aspect ratio (nominal value) of capacitors, there are increased as a consequence of the differential (DNL) and integral (INL) non-linearities, especially large when the number of bits is large. Its solution is to partition each capacitor, connected in parallel similar elements: for example, the nominal value of which is a multiple of  $C_{unit}$ . Parameters are influencing the manufacture of such capacitors, keeping their proportions.

Since the capacitors are charged through the resistance of switches their size should be considered to preserve the accuracy of the DAC

$$\tau = R_{switch}C \rightarrow \frac{T_{CLK}}{2} \gg R256C_{unit} \quad (1)$$

$$\langle V^2 \rangle = \frac{kT}{256C_{unit}} \quad (2)$$

Reducing  $C_{unit}$ , we improves performance (1) DAC, but reduces accuracy: thermal noise (2) is increased and the

effect of parasitic elements on the ratio of the size of capacitors is enhanced.

To reduce the influence of parasitics, wiring elements of the entire array is covered by a grounded metal area (block located above the metal shield), leaving only holes for attachment to the lower plate of the capacitor. This adds more grounded parasitic capacitance from the bottom and top plates, reducing the effect of the parasitic elements of the wiring and increasing consumption at recharging the DAC.

### III. SIMULATION RESULTS AND LAYOUT

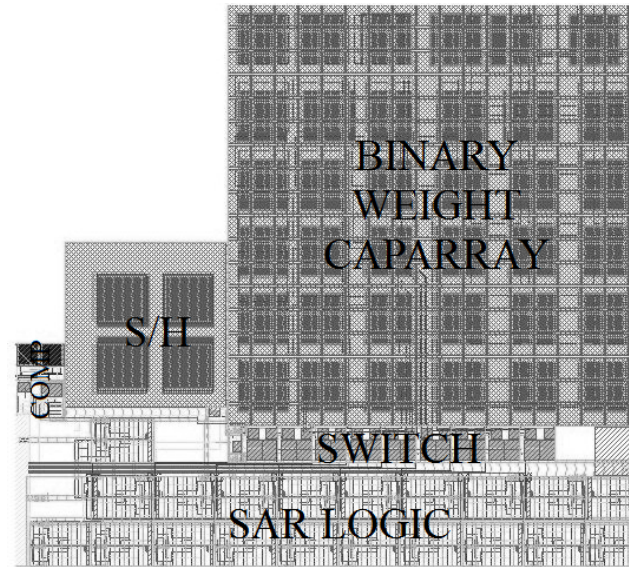


Figure 5: Layout of ADC

The proposed chip was designed for fabrication in a 180 nm single poly 6 metal MMRF CMOS process of UMC (Taiwan). Fig.5 shows the layout of ADC. It occupies chip area including the capacitor array of about  $0.105 \text{ mm}^2$ . Other parameters of the developed ADC are presented in the Table 1.

TABLE I  
PERFORMANCE SUMMARY OF SAR ADC

Parameters	This work
Process	180nm
Resolution	8 b
Chip Area	0.105 mm <sup>2</sup>
Supply	1.8V
Input range	0-1.8V
Sampling rate	20 MS/s
Clock Frequency	200 MHz
ENOB	6,88 b
Power Consumption	2.36 mW
SNDR	43.2 dB

INL and DNL for the designed SAR ADC are shown Fig.6. Accuracy of the DAC is dependent on the accuracy of metal etching and noise in the capacitor array. The peak INL values are between 0.1 to 0.65 LSB and the peak DNL values are -0.55 to 0.68 LSB. Switches with low resistance enhance speed, but increase power consumption and nonlinearity of the ADC.

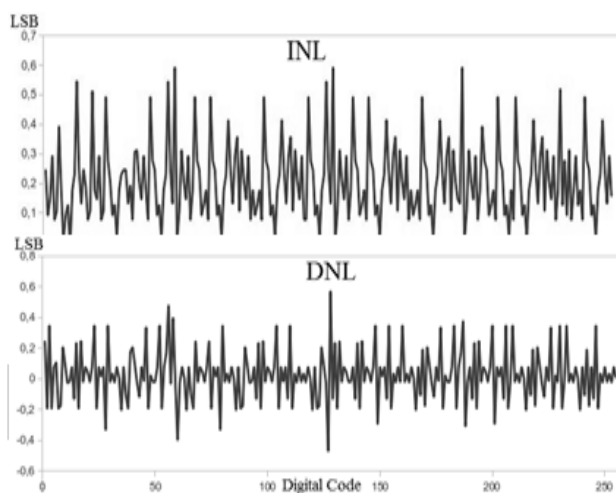


Figure 6: INL and DNL of SAR ADC

#### IV. CONCLUSION

The ADC of Fig.5 designed for the 0.18 μm CMOS technology, occupies on chip area of 325μm x 325μm.

ENOB is 6.88 bits at a sampling frequency of 20 MHz, clock frequency is 200 MHz, SNDR is 43.2 dB. With these parameters the ADC consumes about 1.3 mA at a nominal supply voltage of 1.8V. The designed ADC is considered as a building block for data-driven application specific IC to be developed for muon chamber of the CBM experiment.

#### ACKNOWLEDGEMENT

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