A 12-bit, 200-MS/s, 11.5-mW Pipeline ADC using a Pulsed Bucket Brigade Front-End

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Abstract

A high-speed, low-power pipeline ADC is realized by replacing the front-end residue amplifiers with pulsed bucket brigade circuitry and compensating for the introduced errors using digital linearization. The ADC is implemented in 65-nm CMOS and occupies 0.26 mm^2. It operates at 200 MS/s, consumes 11.5 mW from a 1-V supply and achieves an SNDR of 65 dB at low input frequencies and 57.6 dB near Nyquist. The corresponding SNDR-based Schreier FOM is 164.5 dB and 157 dB, respectively.

Introduction

Most of the power in conventional pipeline ADC stages is consumed by the operational amplifiers that generate the stage residue. In order to reduce the total power of the ADC, new amplification methods are being explored. In [1] a bucket brigade circuit is used to enable efficient residue generation. However, this scheme still relies on auxiliary OpAmps to achieve complete and precise settling, which limits the achievable savings. This work improves upon [1] by eliminating the auxiliary OpAmps and operating the circuit at a low supply voltage in a fine-line process. The residue errors resulting from the removal of the OpAmp are addressed through digital linearization [2].

The core principle used in bucket brigade pipeline stages is charge transfer amplification [3], where charge is moved from a large capacitor to a small capacitor to realize voltage gain. The operation of a conventional OpAmp-boosted bucket brigade circuit [4] is illustrated in Fig. 1(a). During $\phi 1$, the input is sampled on C_{in}, and during ϕ_2 the charge is redistributed onto C_L by forcing a virtual ground at node V_S. With large OpAmp gain, the resulting voltage gain is precisely set to the ratio C_{in}/C_L. The most compelling aspect of this circuit is that the sampled input charge is re-used to charge the output. This is very different from a traditional switched capacitor pipeline, where each stage draws a new charge packet from the supply and its input charge is essentially wasted.

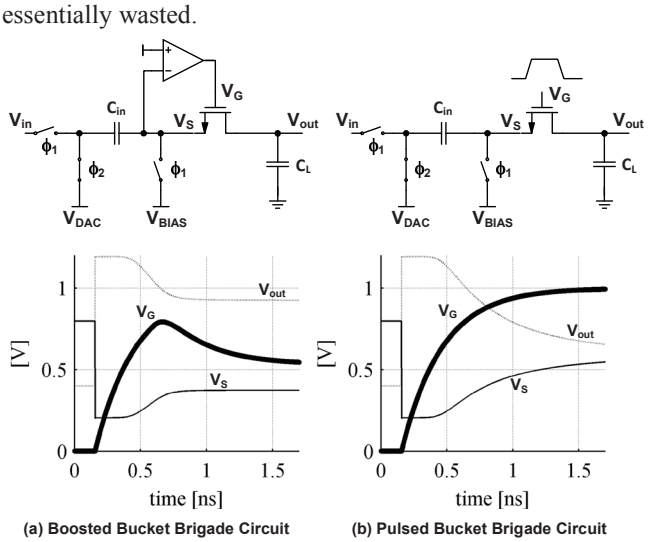

Fig. 1. Conventional and proposed bucket brigade circuit.

Fig. 1(b) shows the proposed OpAmp-less realization. The gate of the pass transistor is driven by a voltage pulse that mimics the behavior of the OpAmp output during the initial transient. Specifically, note that the OpAmp in Fig. 1(a) initially responds with a finite rise time pulse to speed up the charge transfer (bold line labeled V_G). A similar speed-up is achieved in our realization by gating the transistor with a pulse generated by an RC circuit. The main difference between the two circuits is that the OpAmp-less realization does not settle precisely. At the end of ϕ_2, node V_S contains signal dependent linear and nonlinear errors that can drift with temperature (e.g., due to V_t shifts). In the proposed ADC, this issue is mitigated though digital linearization and continuous background calibration.

ADC Architecture and Circuit Design

Fig. 2 shows the block diagram of our 13-stage proof-of-concept design. The first two and most critical stages use the circuit of Fig. 1(b) and are designed for a voltage gain of 3.1. To reduce the calibration overhead, the next three stages are implemented using the OpAmp based topology of Fig. 1(a) with a gain of 2. The 8-stage backend is implemented using traditional 1.5-bit OpAmp-based switched capacitor stages.

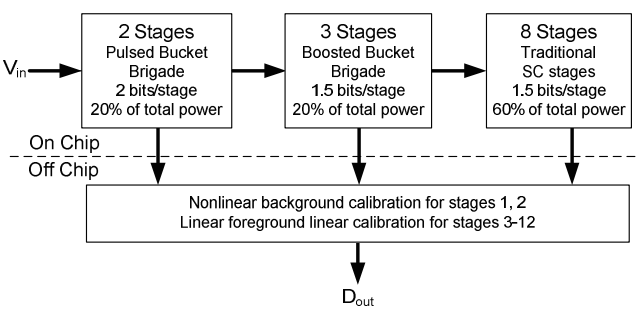

Fig. 2. ADC block diagram.

Fig. 3 shows the half circuit schematic of stage 1. The actual implementation is pseudo-differential and uses two copies of this circuit. The stage is timed in four phases: pre-charge (short phase), sample, compare (short phase) and charge re-distribution.

In the sample phase, the input is sampled in parallel on two equally sized capacitors ($C_{in}/2$). During the compare phase, the top plates of these capacitors are connected to a common mode voltage and the comparators are activated to coarsely quantize the input. In the following redistribution phase, the top plate of one of the sampling capacitors is connected to the reference voltage V_L and the other is connected to its counterpart in the other half circuit. This reduces the common mode gain to unity and thus allows us to cascade pseudo-differential stages without significant common-mode deterioration from stage to stage.

The DAC capacitances are charged to the reference voltages during the sample phase. During redistribution, the DAC switches are set according to the comparator decisions and V_G is pulsed for fast charge transfer to the next stage, as

explained above. Since the input of stage 1 is a voltage, the pre-charge phase is not used. In stages 2-5, which operate on input charge, the pre-charge phase serves to initialize the input node voltage prior to receiving charge from its driving stage.

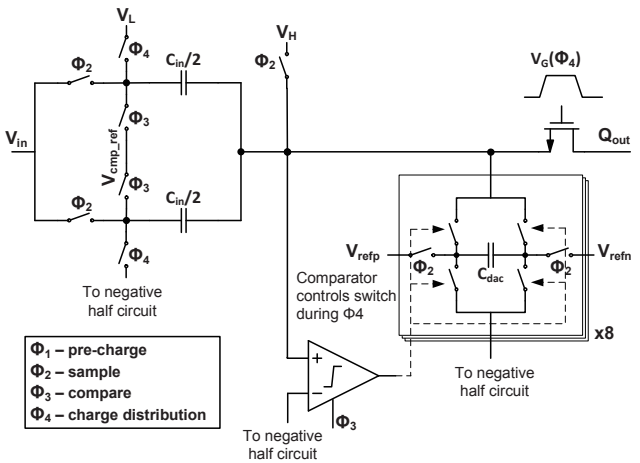

Fig. 3. Implementation of the first pipeline stage.

Measurement Results

A prototype IC was implemented in 65-nm CMOS. The total die area is 3.33 mm^2 and the ADC core occupies 0.26 mm^2 (see Fig. 4). As indicated in Fig. 2, the calibration is performed off-chip on full-speed output data. For realistic results, the calibration engine is run once using low-frequency inputs and the coefficients remain frozen as the input frequency is swept. Fig. 5 shows the measured results, which indicate an SNDR of 65 dB at low input frequencies (f_{in} = 1 MHz) and 57.6 dB near Nyquist (f_{in} = 99 MHz). The high-frequency degradation is in part due to clock jitter, which was estimated to about 1.2 ps_{rms} in our setup. Fig. 6 shows the measured DNL and INL, which are within 1 and 1.25 LSB, respectively, at the 12-bit level.

With P = 11.5 mW (excluding reference, I/O and external calibration engine), The achieved SNDR-Schreier FOM = $SNDR_{dB} + 10\log[(f_s/2)/P]$ is 164.5 dB for low f_{in} and 157 dB near Nyquist. The design therefore achieves leading edge power efficiency at the given speed while providing higher resolution than competing high-speed OpAmp-less topologies, such as [5].

Acknowledgements

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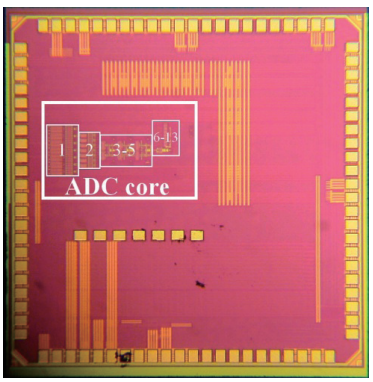

Fig. 4. Die photograph.

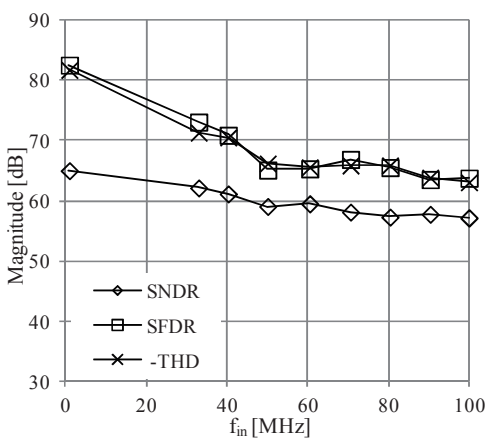

Fig. 5. SNDR, SFDR and -THD vs. f_{in} (f_s=200 MHz).

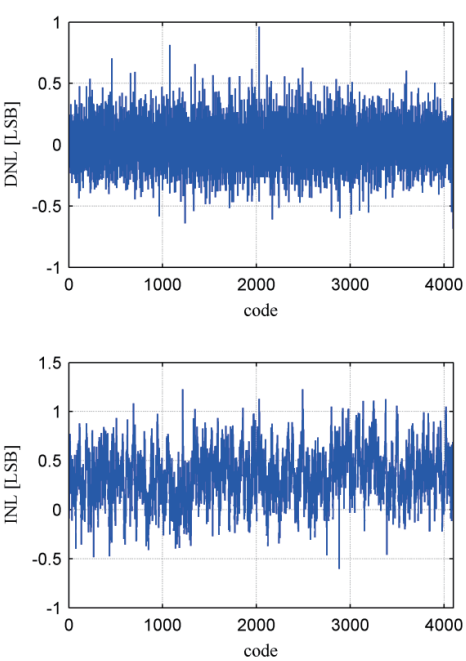

Fig. 6. Measured DNL and INL (f_s=200 MHz).