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Fabrication of pseudo-spin-MOSFETs using a multi-project wafer CMOS chip

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ABSTRACT

We demonstrate monolithic integration of pseudo-spin-MOSFETs (PS-MOSFETs) using vendor-made MOSFETs fabricated in a low-cost multi-project wafer (MPW) product and lab-made magnetic tunnel junctions (MTJs) formed on the topmost passivation film of the MPW chip. The tunneling magnetoresistance (TMR) ratio of the fabricated MTJs strongly depends on the surface roughness of the passivation film. Nevertheless, after the chip surface was atomically flattened by SiO_2 deposition on it and successive chemical–mechanical polish (CMP) process for the surface, the fabricated MTJs on the chip exhibits a sufficiently large TMR ratio (>140%) adaptable to the PS-MOSFET application. The implemented PS-MOSFETs show clear modulation of the output current controlled by the magnetization configuration of the MTJs, and a maximum magnetocurrent ratio of 90% is achieved. These magnetocurrent behaviour is quantitatively consistent with those predicted by HSPICE simulations. The developed integration technique using a MPW CMOS chip would also be applied to monolithic integration of CMOS devices/circuits and other various functional devices/materials, which would open the door for exploring CMOS-based new functional hybrid circuits.

1. Introduction

CMOS/Spintronics hybrid technology has attracted considerable attention for low power logic systems [1–13]. In particular, pseudo-spin-MOSFETs (PS-MOSFETs) are promising for energy-efficient CMOS logic systems based on nonvolatile power-gating architecture [4–9]. The PS-MOSFET is a new class of spin-transistor consisting of an ordinary MOSFET and a magnetic tunnel junction (MTJ), which can be easily realized by the present MRAM (spin RAM) technology. This device can exhibit high and low current drivabilities controlled by the magnetization configuration (parallel (P) or antiparallel (AP)) of the MTJ [4], which is a promising feature for nonvolatile logic applications such as nonvolatile bistable circuits [3]. Nonvolatile SRAM (NV-SRAM) and nonvolatile flip–flop (NV-FF) are essential circuits for nonvolatile power-gating architecture, and these circuits can be configured with PS-MOSFETs [5–9]. The operation, performance, and design of PS-MOSFETs have been systematically investigated using HSPICE simulation [7]. Moreover, the basic operations of PS-MOSFETs were experimentally demonstrated by fabrication of a prototype PS-MOSFET using a lab-made bottom-gated SOI MOSFET and MTJ [10] and hybrid integration of a PS-MOSFET using a vendor-made MOSFET and a lab-made MTJ [7].

In this paper, we demonstrate monolithic integration of PS-MOSFETs using a custom CMOS chip fabricated through multi-project wafer (MPW) service. The implemented PS-MOSFETs using this technique show excellent spin-transistor characteristics with high magnetocurrent ratios, which are consistent with HSPICE simulation predictions. In this technique, high-performance MOSFETs are easily available at a low cost, and we can freely design the size and layout of MOSFETs. Furthermore, new functional devices/materials could be integrated on a MPW CMOS chip by introducing post-chip-manufacturing integration technique. These features are beneficial to explore heterogeneous integration of CMOS and new functional devices/materials.

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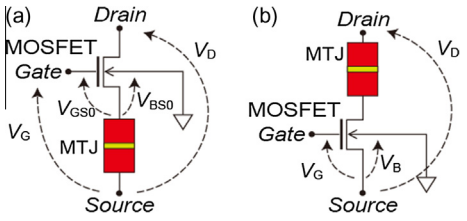

Fig. 1. Circuit configurations of (a) a pseudo-spin MOSFET (PS-MOSFET) and (b) a MOSFET with drain-side MTJ connection.

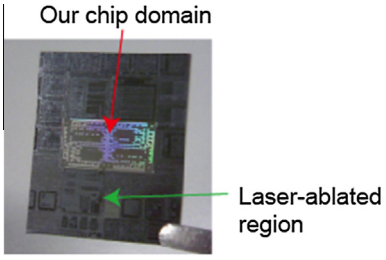

Fig. 2. Photograph of the MPW CMOS chip.

2. Fabrication process of PS-MOSFETs

Fig. 1(a) shows the circuit configuration of the PS-MOSFET, in which the source terminal of the ordinary MOSFET is connected to the MTJ. Since the voltage drop of the MTJ negatively feedbacks to the gate and body biases, the effective biases V_{GS0} and V_{BS0} for the ordinary MOSFET can be varied by the resistance state of the connected MTJ. As a result, the PS-MOSFET can exhibit spin-transistor characteristics: The high and low current drivabilities can be achieved depending on the magnetization configuration (P or AP) of the MTJ [3].

Fig. 2 shows a MPW CMOS chip used for implementation of PS-MOSFETs. The chip was cut into a larger size than our chip domain to adapt the chip die to our lithography alignment system. The surround region of our chip domain (which was designed by other projects/customers) was laser-ablated for inactivation by the vendor, and this region had agglomeration structures with ~2 μm in height. Fig. 3 shows the fabrication process flow of a PS-MOSFET using a MPW CMOS chip. First, a 200-nm-thick SiO_2 layer was covered over the entire chip for protection of the chip

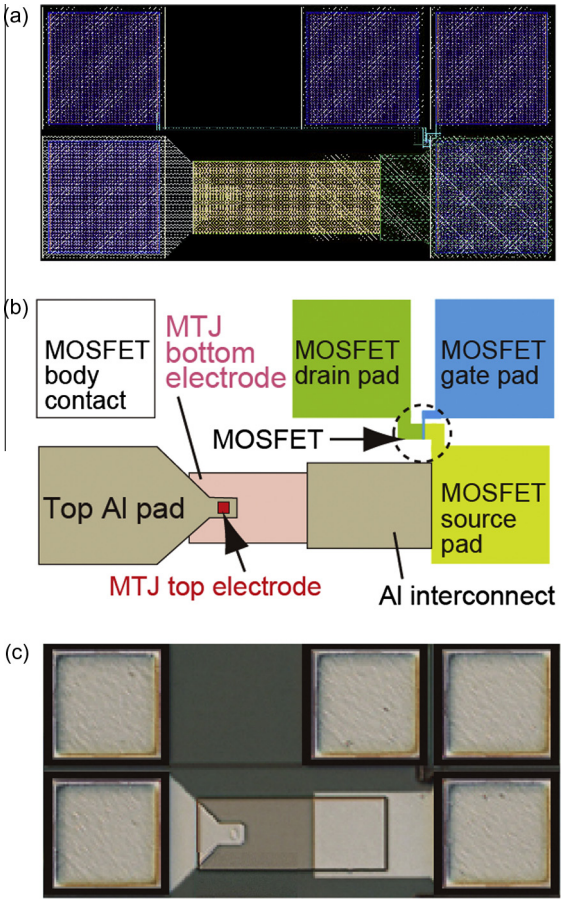

Fig. 4. (a) Layout design, (b) its schematic illustration and (c) a micrograph of a fabricated PS-MOSFET .

(in particular, for the protection of the contact pads of MOSFETs fabricated in the MPW chip) during the successive MTJ process, in which the SiO_2 film was deposited by a ECR-plasma-enhanced sputtering system. Then, the laser-ablated region was rasped, and the surface was subsequently flattened by chemical–mechanical polish (CMP) with colloidal silica slurry (pH ~ 7). To remove debris particles on the surface, the chip was completely cleaned by cyclic repetition of mega-sonic DI water treatment and successive O_2

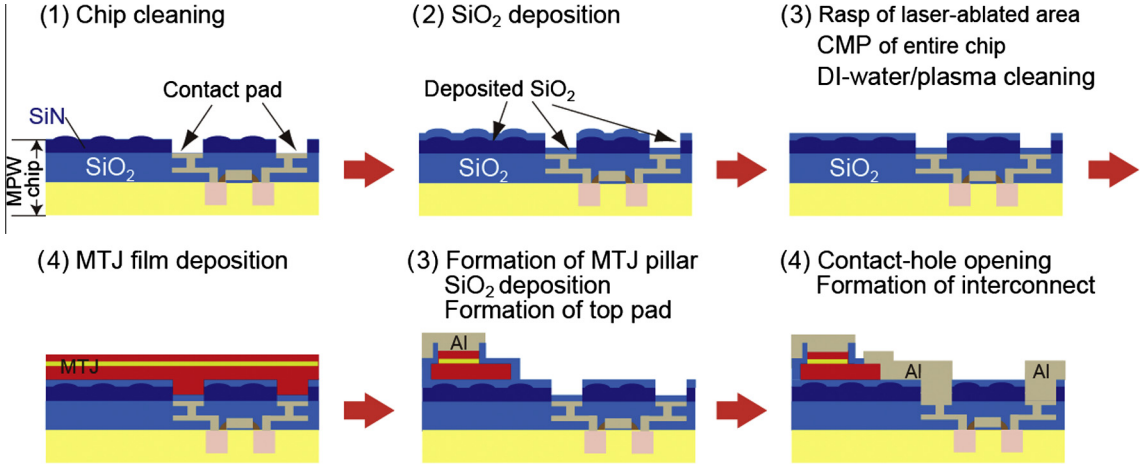

Fig. 3. Fabrication process flow of a PS-MOSFET.

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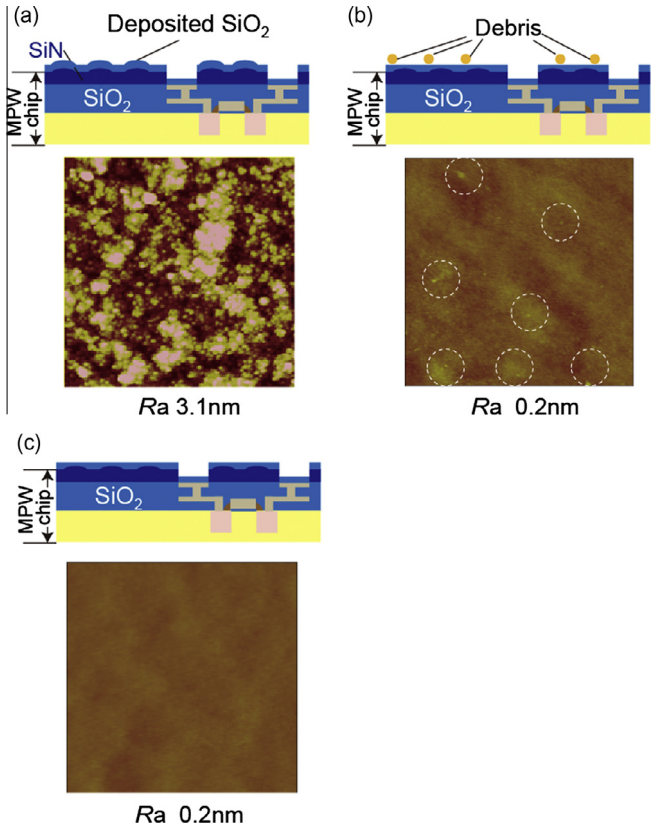

Fig. 5. AFM images of the chip after (a) SiO_2 deposition, (b) CMP flattening and (c) successive cleaning using megasonic DI water treatment and O_2 plasma exposure. Debris particles after the CMP flattening are indicated by dotted circles in (b). The AFM scan area is 1 μm × 1 μm.

plasma exposure. After a film stack for MTJs was deposited on the surface, the film stack was processed into pillar-shaped MTJs using UV lithography and Ar ion milling. Then, the surface of the MTJs was covered with a SiO_2 film for passivation, and an Al contact pad for the top electrode of each MTJ was formed. The bottom electrode of the MTJ and the source contact pad of a MOSFET were connected with an Al interconnect. Finally, an Al contact pad for the drain contact pad of the MOSFET was formed. Fig. 4(a)–(c) shows the layout design of a PS-MOSFET, its schematic illustration, and a photograph of the fabricated PS-MOSFET.

3. Surface flattening of a MPW chip

In this study, Heusler-alloy-based MTJs having the film stack of Ru/IrMn/CoFe/MgO/Co_2FeAl/Cr/MgO/SiO_2 were used for the PS-MOSFET fabrication. This type of MTJ can exhibit a high tunnel magnetoresistance (TMR) ratio (166%), when it is formed on an atomically flat SiO_2 surface [14]. Therefore, the surface planarization and cleaning processes of the MPW chip would be highly important to obtain a high TMR ratio.

Fig. 5(a) shows the AFM image of a 200-nm-thick SiO_2 layer deposited on the top of a MPW chip. The mean surface roughness (*Ra*) of this surface was ~3.1 nm that was almost the same as that of the SiN passivation surface of the original MPW chip, i.e., the surface roughness was not improved by the SiO_2 deposition. When MTJs were formed on this surface, the TMR ratio was degraded to 20%. Fig. 5(b) shows the AFM image of the chip surface after the SiO_2 passivation film was flattened by CMP. Although the surface became atomically flat (*Ra* = ~0.2 nm), there were residual debris particles on the surface after the chip was cleaned by typical method (ultra-sonic cleaning with DI water and acetone). These debris particles also lowered the TMR ratio of MTJs fabricated on the surface. To remove the debris particles, the chip was cleaned

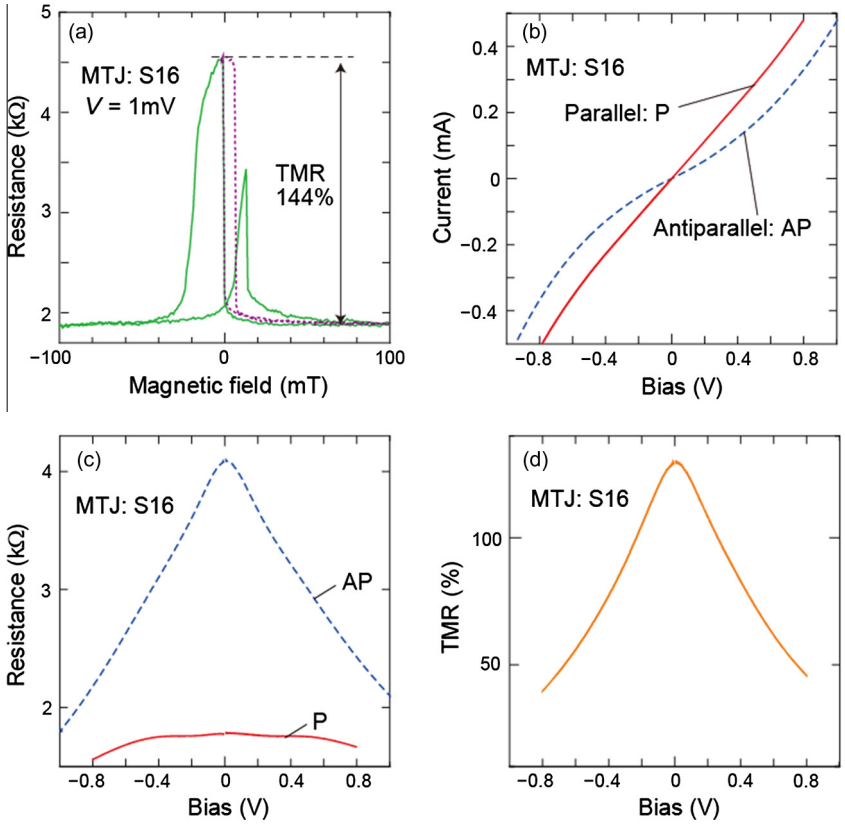

Fig. 6. (a) Magnetic-field dependence of junction resistance, (b) *I–V* characteristics, (c) *R–V* characteristics and (d) bias dependence of TMR for a fabricated S16 MTJ. Solid and dotted curves in (a) represent major and minor loops, respectively.

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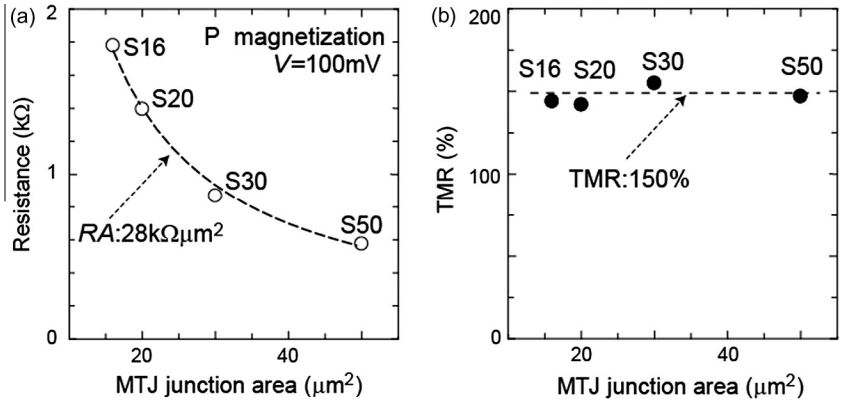

Fig. 7. (a) Junction resistance as a function of junction area and (b) TMR as a function of junction area for fabricated S16–S50 MTJs.

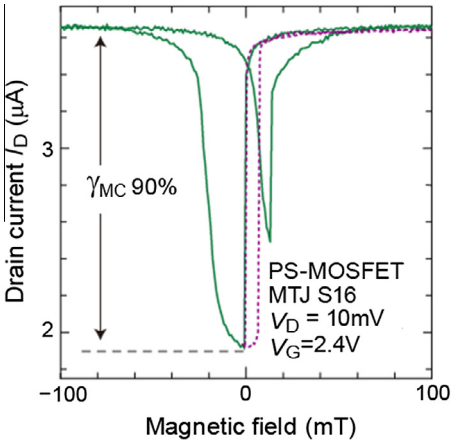

Fig. 8. Magnetocurrent characteristics of a fabricated PS-MOSFET using the S16 MTJ. Solid and dotted curves represent major and minor loops, respectively.

by cyclic repetition of mega-sonic DI water treatment and successive O_2 plasma exposure as described above. Fig. 5(c) shows the AFM image of the chip surface after this cleaning process. The atomically flat surface (Ra = ~0.2 nm) without debris particles was achieved. MTJs fabricated on this surface exhibited a large TMR ratio of ~150%.

4. Characteristics of fabricated MTJ

MTJs with different cross-sectional sizes of 16, 20, 30, and 50 μm^2 were fabricated on the atomically flattened and completely cleaned surface of a MPW chip. Hereafter, these are referred to as S16, S20, S30, and S50, respectively. All the measurements were performed at room temperature. The magnetoresistance effects of the MTJs were evaluated from their TMR ratios that were defined by $(R^{AP}–R^{P})/R^{AP}$ using the MTJ resistances R^{P} and R^{AP} in the P and AP magnetization configurations, respectively. Fig. 6(a) shows the TMR ratio of the S16 MTJ as a function of magnetic field, measured with a bias of 1 mV. The solid and dotted curves represent major and minor loops, respectively. The clear hysteresis behaviour in the major loop originates from the P- to -AP and AP- to -P magnetization switching of the MTJ. This behaviour is also seen in the minor loop shown by the dotted curve in the figure. The maximum TMR ratio is 144%. Fig. 6(b) and (c) shows the I–V and R–V characteristics of the S16 MTJ in the P and AP magnetization configurations, respectively. The bias dependence of the TMR ratio is also shown in Fig. 6(d). The bias voltage (V_{half}) when the TMR ratio is reduced to half its original value is 0.4 V.

Fig. 7(a) and (b) shows the junction resistance and the maximum TMR ratio of the S16–S50 MTJs as a function of junction area, respectively. All the MTJs showed a single RA value of ~28 kΩ μm^2 and a TMR ratio of ~150%. These are consistent with the current in-plane tunneling (CIPT) measurement result for the MTJ film stack prior to the MTJ pillar fabrication, indicating excellent controllability of our fabrication process.

5. Integration of PS-MOSFETs and their characteristics

PS-MOSFETs were integrated by the above-described process using S16–S50 MTJs and vendor-made MOSFETs with W/L = 2 μm/350 nm. Output and magnetocurrent characteristics of the fabricated PS-MOSFETs were measured at room temperature.

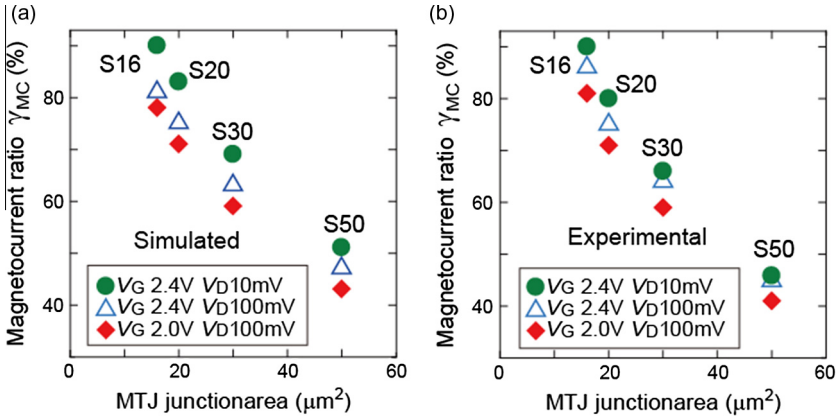

Fig. 9. (a) Simulated γ_{MC} and (b) experimentally-measured γ_{MC} as a function of junction area for fabricated PS-MOSFETs using S16–S50 MTJs.

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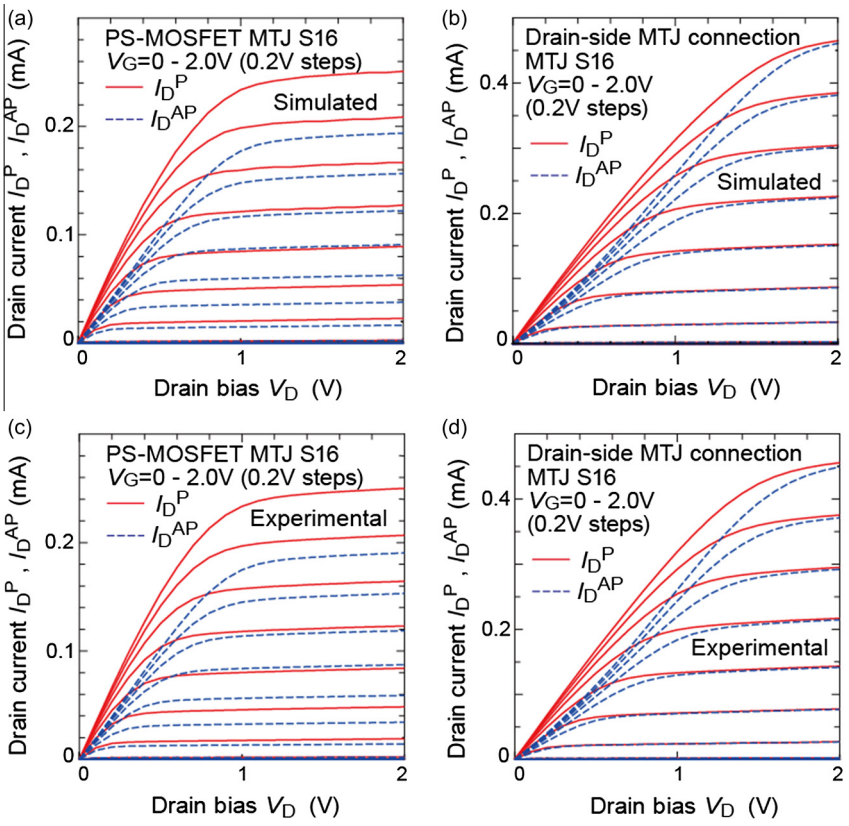

Fig. 10. Simulated I_D–V_D characteristics of (a) the PS-MOSFET with S16 MTJ and (b) a MOSFET with drain-side S16 MTJ. Experimentally-measured I_D–V_D characteristics of (c) the PS-MOSFET with S16 MTJ and (d) the MOSFET with drain-side S16 MTJ.

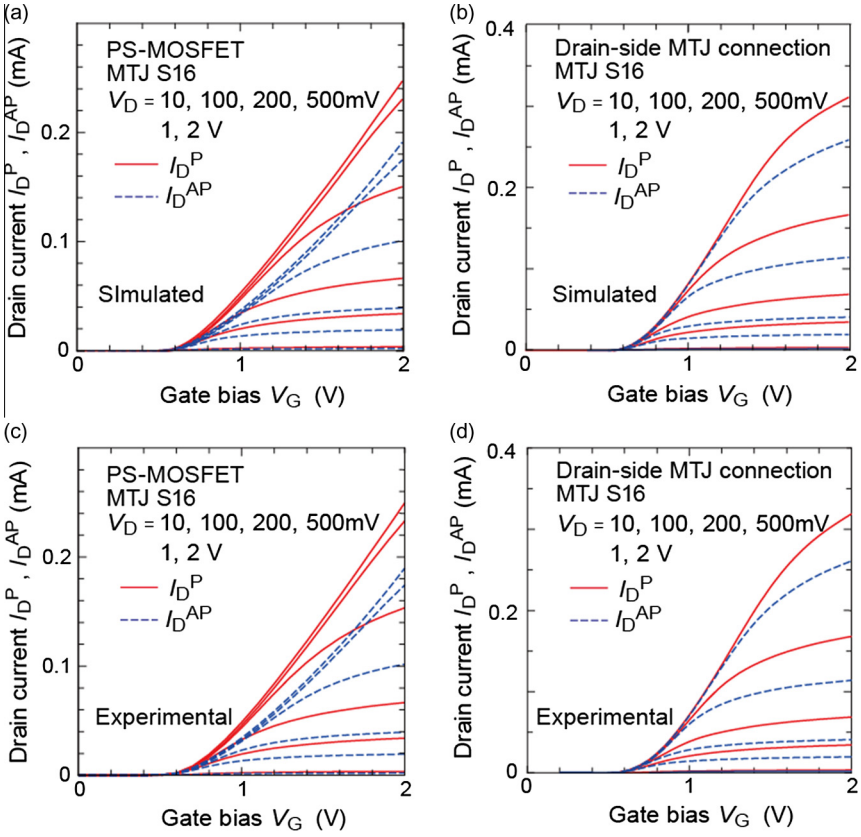

Fig. 11. Simulated I_D–V_G characteristics of (a) the PS-MOSFET with S16 MTJ and (b) the MOSFET with drain-side S16 MTJ. Experimentally-measured I_D–V_G characteristics of (c) the PS-MOSFET with S16 MTJ and (d) the MOSFET with drain-side S16 MTJ.

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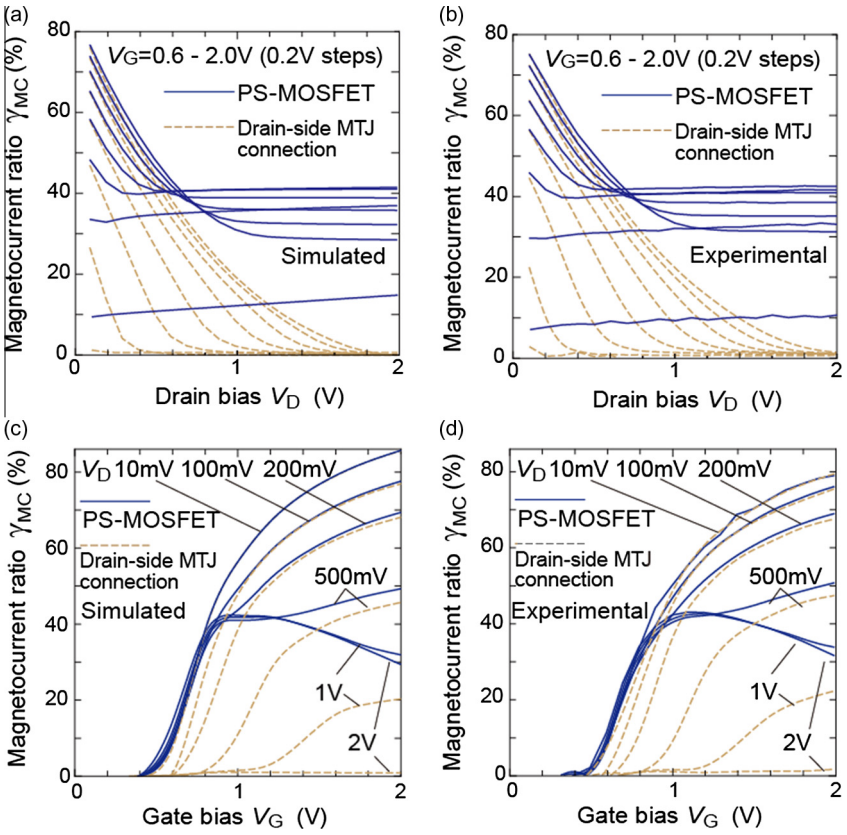

Fig. 12. (a) Simulated γ_{MC} and (b) experimentally-measured γ_{MC} as a function of V_D for the PS-MOSFET with S16 MTJ and the MOSFET with the drain-side S16 MTJ. (c) Simulated γ_{MC} and (d) experimentally-measured γ_{MC} as a function of V_G for the PS-MOSFET with S16 MTJ and the MOSFET with the drain-side S16 MTJ.

Fig. 8 shows the magnetocurrent characteristics of the PS-MOSFET using the S16 MTJ for V_D = 10 mV and V_G = 2.4 V, where the solid and dotted curves represent major and minor loops, respectively. The measured drain currents for both the major and minor loops showed clear hysteresis characteristics that were caused by those of the MTJ (see Fig. 6(a)). The magnetocurrent ratio γ_{MC} is given by ($\gamma_{MC} = I_D AP - I_D^P/I_D^{AP}$), in which I_D^P and I_D^{AP} represent the drain currents in the P and AP magnetization configurations, respectively. A high γ_{MC} of 90% was achieved, as shown in the figure, which is the highest γ_{MC} for previously-reported MOSFET-type spin-transistors. Fig. 9(a) shows simulated γ_{MC} as a function of MTJ junction area. γ_{MC} can be controlled by the resistance of the MTJs, since the negative feedback effect is enhanced by increasing MTJ resistance. This behaviour was experimentally confirmed, as shown in Fig. 9(b).

Fig. 10(a) shows simulated I_D–V_D characteristics for the PS-MOSFET using the S16 MTJ. The ideal spin-transistor behaviour, i.e., the different current drivabilities of I_D^P and I_D^{AP}, was predicted to clearly appear. Fig. 10(b) shows simulated I_D–V_D characteristics for a MOSFET with drain-side MTJ connection (that has no negative feedback effect, as shown in Fig. 1(b)). In this case, the difference between I_D^{AP} and I_D^P is reduced by increasing V_D in contrast to the PS-MOSFET. These I_D–V_D characteristics for the two circuit configurations were experimentally observed using the fabricated devices, and the measured results are quantitatively consistent with the simulated results, as shown in Fig. 10(c) and (d). Fig. 11(a) and (b) shows simulated I_D–V_G characteristics for both the circuit configurations. The current drivability of the PS-MOSFET is lower than that of the MOSFET with the drain-side MTJ connection, which is due to the negative feedback effect of the PS-MOSFET. However, this demerit can be excluded for bistable circuit applications of PS-MOSFETs [7]. The predicted I_D–V_G characteristics for the two circuit configurations were experimentally observed using the fabricated devices, as shown in Fig. 11(c) and (d).

Fig. 12(a) shows simulated γ_{MC} as a function of V_D for the PS-MOSFET and the MOSFET with the drain-side MTJ connection. The γ_{MC} characteristics are quite different for both the circuit configurations. γ_{MC} for the PS-MOSFET saturates at a relatively high value for higher V_D. This is because the negative feedback effect can suppress the voltage drop of the MTJ to a relatively low value and thus the bias-dependent TMR characteristics are hidden [7]. On the other hand, γ_{MC} for the other circuit configuration decreases with increasing V_D. These γ_{MC} characteristics were completely reproduced using the fabricated device, as shown in Fig. 12(b). Furthermore, the simulated V_G-dependent γ_{MC} characteristics are also identical to the experimental observations, as shown in Fig. 12(c) and (d).

As demonstrated here, the magnetocurrent characteristics of the PS-MOSFETs can be accurately predicted using the HSPICE simulation technique, and these characteristics can be reproduced by the monolithic integration of the PS-MOSFETs using a MPW CMOS chip.

6. Conclusion

We have developed the monolithic integration technique of PS-MOSFETs using a low-cost MPW CMOS chip and demonstrated the spin-transistor characteristics of the fabricated PS-MOSFETs that were predicted by HSPICE simulations. The developed integration technique using a MPW CMOS chip would also be applied to monolithic integration of CMOS devices/circuits and other various functional devices/materials, leading to a new route to more-than-Moore research.

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