Dual-Gate MoS_2 FET With a Coplanar-Gate Engineering

Jie Jiang, Ayayi C. Ahyi, and Sarit Dhar

***Abstract*— A dual-gate multilayer MoS_2 FET with a standard backside gate and a nonstandard coplanar top gate is demonstrated and analyzed. The special feature of this device is that the gate and MoS_2 channel can be directly coupled on the same plane through the bottom-conducting Si substrate. The coplanar-gate MoS_2 FET shows a good performance with a large ON–OFF ratio ($I_{ON/OFF}$) of 1.5×10^4, a small subthreshold swing (S) of 0.13 V/decade, and a field-effect mobility (μ) of 0.69 cm^2/Vs, respectively. Furthermore, a large V_{th} modulation (−0.55∼6.4 V) can be obtained in a dual-gate MoS_2 FET by changing the coplanar-gate bias, which makes the device switch from depletion-mode to enhancement-mode operation, without affecting μ and S, regardless of the coplanar-gate bias. In such a dual-gate MoS_2 FET, both top and bottom gates can share the same SiO_2 dielectric, and the deposition of source/drain/gate contact can be combined to a single step. A band diagram with the body effect theory is proposed to explain the device operation mechanism. The coplanar-gate MoS_2 FET with its dual-gate operation and simple fabrication process can provide a good candidate for low-cost 2-D planar nanoelectronics and sensor applications.**

***Index Terms*— 2-D MoS_2, coplanar gate, dual gate, FETs, threshold voltage.**

I. Introduction

2-D SEMICONDUCTORS such as MoS_2 have attracted significant interests as layered transition-metal dichalcogenide semiconductors due to their unique electronic, optical, and mechanical properties [1], [2]. 2-D MoS_2-based FETs show a promising future for many applications, such as photonic detectors [3], ICs [4], and chemical sensors [5]. To explore more functionalities, a dual-gate MoS_2 FET configuration was proposed as a powerful tool, because the second gate can provide an additional gate control to the MoS_2 channel [6], [7]. Recently, different groups have demonstrated pioneering works by using dual-gate MoS_2 FET configurations. For example, Radisavljevic *et al.* [6] reported the metal–insulator transition in MoS_2 by using a dual-gate device configuration with HfO_2 top dielectric capping. Tarasov *et al.* [7] optimized the mobility of MoS_2 by electrostatic doping in a dual-gate MoS_2 FET with Al_2O_3 top dielectric. More recently, Roy *et al.* [8] successfully fabricated tunnel diodes and transistors by using a dual-gate MoS_2 FET with ZrO_2 top dielectric capping [8]. The dual-gate MoS_2 device structures are usually based on the MoS_2 channel sandwiched between two gate electrodes from which it is electrically isolated by two different gate dielectrics.

From a fabrication perspective, a simpler process with fewer steps is attractive for improving the device yield and reducing the fabrication cost. Recently, an interesting approach was proposed by using side-gate coplanar configuration for GaAs-based high-electron-mobility transistors [9]–[12]. Based on this architecture, the deposition of gate, source, and drain can be completed on the same plane using a one-step process, which greatly simplifies the device processing. This kind of FET has been demonstrated to show promise in high-speed photodetector and logic device applications [9]–[12]. Furthermore, it is to be noted that, in the recent 2-D FET (MoS_2, graphene) domain, some groups have also reported that the coplanar-gate MoS_2 or graphene FET can be realized by using a top-gate polymer electrolyte or ionic liquid, which connects the gate electrode and 2-D channel in the same plane directly [13]–[16]. Kim *et al.* [13] demonstrated a coplanar-gate transparent 2-D graphene transistor for logic circuits on flexible plastic substrate and pressure sensor matrix application [14]. Using this coplanar-gate 2-D FET configuration, Lin *et al.* [15] recently reported an improved carrier mobility in a coplanar-gate MoS_2 FET by using organic ionic liquid as the top dielectric [15]. Ye *et al.* [16] successfully demonstrated superconductivity in the multilayer MoS_2 coplanar-gate FET by using top ionic-liquid dielectric [16]. Although these devices show high promise for some important applications, the organic nature of these materials raises concerns about severe device instability under operating conditions.

In this paper, we demonstrate a coplanar-gate multilayer MoS_2 FET without any top dielectric. To the best of our knowledge, for the first time, we find that the MoS_2 channel and a coplanar gate can be directly coupled by the bottom-conducting Si substrate. Based on this configuration, a dual-gate MoS_2 FET is demonstrated by coupling MoS_2 channel and coplanar gate on the same plane directly. The threshold voltage (V_{th}) of this device can be tuned from −0.55 to 6.4 V by modulating the coplanar-gate bias from 20 to −15 V. Compared with the traditional dual-gate MoS_2 FET, this device has the following advantages.

1) Top gate and bottom gate share the common SiO_2 dielectric.
2) The source, drain, and coplanar gate can be deposited in one-step process within the same plane.

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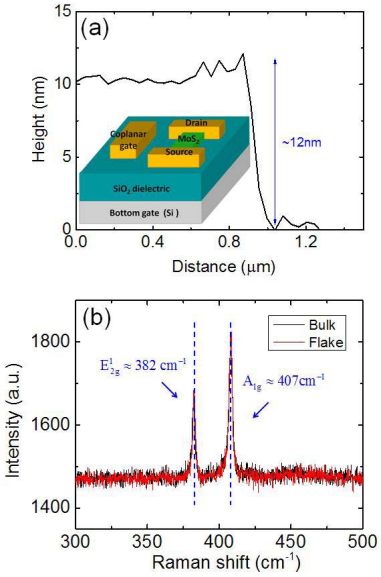

Fig. 1. (a) Height measurement using AFM at the MoS_2 flake edge. Inset: schematic of the coplanar-gate MoS_2 FET. (b) Raman spectra of MoS_2 flake and bulk MoS_2.

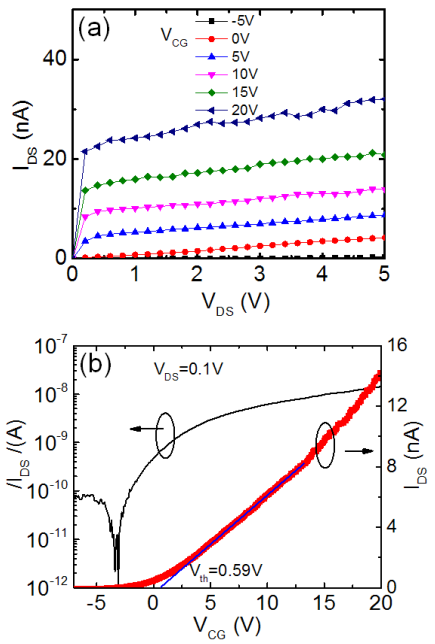

Fig. 2. (a) Output characteristics of coplanar-gate MoS_2 FET. (b) Transfer characteristic of a coplanar-gate MoS_2 FET obtained by sweeping the V_{CG} from -7 to 20 V with a fixed bias of $V_{DS} = 0.1$ V. V_{CG}: coplanar-gate voltage.

This new gate-engineering method and fabrication approach for MoS_2 FET may provide a new route to realize 2-D planar-integrated nanoelectronics.

II. Experimental Details

MoS_2 flakes were exfoliated from a bulk crystal by mechanical cleavage and subsequently transferred to a highly doped Si substrate with a 290-nm SiO_2 capping layer. The gate, source, and drain electrodes (Ti/Cr/Au: 20/20/130 nm) were patterned by photolithography/liftoff, where the metals were deposited by dc-sputtering. The thickness of MoS_2 flakes was measured by atomic force microscopy (AFM). Raman spectroscopy, employing a Kimmon Electric HeCd laser as the excitation source, was used to evaluate the chemical quality of the flakes. Capacitance–voltage (C–V) characteristics of the devices were measured by Keithley 590 CV analyzer, and current–voltage characteristics were measured by Keithley2400 SMUs in the dark at room temperature.

III. Results and Discussion

Fig. 1(a) (inset) shows a schematic of the device. The experiment details can be found in the experimental section at the end of the main text. The thickness and chemical nature of exfoliated MoS_2 flakes were measured by AFM and Raman spectroscopy, respectively. Fig. 1(a) shows the profile line information from the AFM measurement for the exfoliated MoS_2 flake with a thickness of ~12 nm. Based on a 0.65-nm thickness per layer value according to [1] and [2], we estimate that the thickness of this MoS_2 flake is ~18 layers. Fig. 1(b) shows the Raman spectra of a sample tested in dark and air ambient environment. In-plane E^1_{2g} mode (~382 cm^{-1}) and out-of-plane A_{1g} mode (~407 cm^{-1}) are observed in both thin MoS_2 flake and bulk MoS_2 flake [17]. That is to say, the Raman spectrum of the MoS_2 flake is very similar to that of the bulk MoS_2 flake, indicating good crystalline characteristic and negligible structural modifications in the exfoliated flake [18].

The output and transfer characteristics of coplanar-gate MoS_2 FET can be summarized in Fig. 2(a) and (b), respectively. The output curve is measured by sweeping the values of V_{DS} from 0 to 5 V with a fixed coplanar-gate V_{CG} from -5 to 20 V, with 5 V steps. From the output curve, good linear characteristics in the low V_{DS} and pinchoff characteristics in the high V_{DS} regimes were observed, indicating consistence with the traditional FET theory. The transfer curve was obtained by sweeping the coplanar-gate voltage from -7 to 20 V with a fixed $V_{DS} = 0.1$ V (here, the bottom gate is floating). A large ON–OFF ratio ($I_{ON/OFF}$) and a small subthreshold swing (S) were found to be 1.5×10^4 and 0.13 V/decade, respectively. This is only for a proof-of-concept for a coplanar MoS_2 transistor. To get a stronger coupling between the coplanar gate and the channel, further work needs to be done to improve the device performance, like choosing a large width-to-length ratio (W/L), using a high-k dielectric, etc. A near-zero threshold voltage ($V_{th} = 0.59$ V) was extracted by extrapolating the linear portion of I_{DS}–V_{GS} curve (as shown in the right linear scale axis) to a zero drain current.

C–V measurements can be used to understand the operation mechanism of a coplanar-gate MoS_2 FET and calculate the field-effect mobility (μ). Using the same silicon wafer with the same oxide, we confirmed that two electrodes deposited on top of the oxide remain capacitively coupled independently of the distance separating them. Fig. 3 shows the C–V measurements (probe frequency: 100 kHz) as a function of coplanar-electrode voltage with different electrode distances (from 10 to 80 μm, step = 10 μm). A constant value (~0.3 pF) was observed from this figure during sweeping the coplanar-electrode voltage

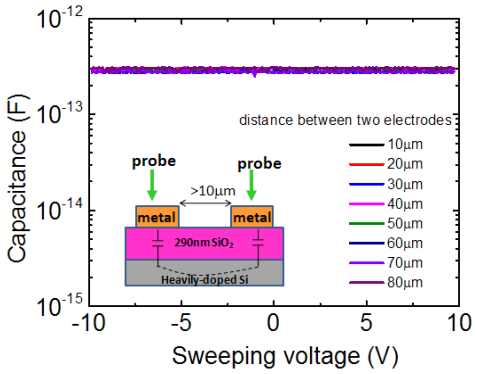

Fig. 3. C–V measurements as a function of coplanar-electrode voltage with different electrode distances (from 10 to 80 μm, step = 10 μm).

from −10 to 10 V. In particular, the capacitance values were almost unchanged with the electrode distance increasing from 10 to 80 μm. It should be noted that, the previous report has shown that the constant C–V value may be due to screening of the electric field by the highly doped Si layer underneath [19]. The invariance of the capacitance with the change in the electrode distance may indicate that only the capacitance of one of the electrodes and the underlying Si layer matters [19].

Based on the C–V results and the data presented in Fig. 3(b), we calculate the values of μ from the linear region of the transfer curve (I_{DS}–V_{GS}) according to the equation [20]

$$\mu = \frac{L}{W \times C_{coplanar} \times V_{DS}} \times \frac{dI_{DS}}{dV_G} \quad (1)$$

where $L = 5$ μm is the channel length, $W = 8$ μm is the channel width, and $C_{coplanar} = 5.85$ nF/cm^2 is the SiO_2 dielectric unit capacitance (considering that they are laterally coupled, they are separated by twice the oxide thickness). The field-effect mobility of the device is thus calculated to be 0.69 cm^2/Vs. It should be noted that this value is underestimated as it does not include the effect of contact resistance between the source/drain metals and MoS_2 and the effect of depletion zone in the Si. Changing the present source/drain metal to Scandium may improve the field-effect mobility of our device as suggested in a recent report [21].

Next, a dual-gate operation of the device with coplanar-gate configuration was characterized. The transfer characteristics in the linear region ($V_{DS} = 0.1$ V) was measured by sweeping the bottom-conducting Si electrode (V_{BG}) with different coplanar-gate biases (V_{CG} from −15 to 20 V, step = 5 V), as shown in Fig. 4(a). From this figure, it is clear that positive coplanar-gate voltages make the transfer curves shift toward negative gate-voltages, whereas for negative coplanar-gate voltage, the transfer curve shifts in the opposite direction. The V_{th} value of a dual-gate MoS_2 FET with different coplanar-gate biases was calculated by extrapolating the linear portion of I_{DS}–V_{GS} curve to a zero drain current, as shown in Fig. 4(b). It was found that the dual-gate MoS_2 FET has a large V_{th} modulation (−0.55 to 6.4 V) when the coplanar-gate bias is changed from 20 to −15 V, which results in a turnaround from the depletion-mode operation to the enhancement-mode operation.

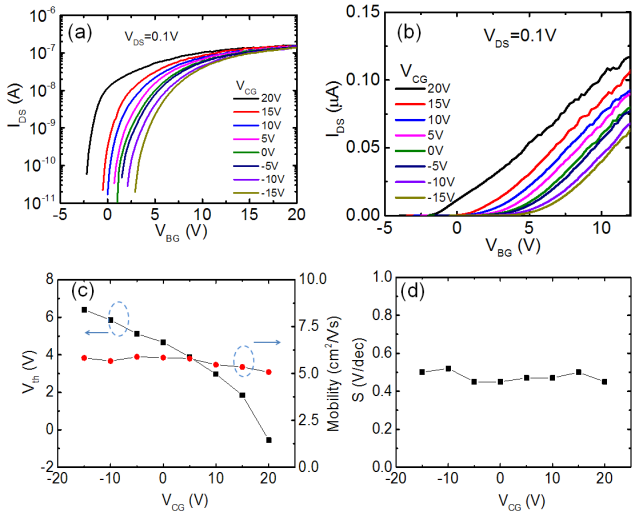

Fig. 4. (a) Transfer characteristics in the linear region ($V_{DS} = 0.1$ V), obtained by sweeping the bottom-conducting Si electrode with different values of V_{CG} (from −15 to 20 V, step = 5 V). (b) Extracted V_{th} values obtained by extrapolating the linear portion of I_{DS}–V_{GS} curve to a zero drain current. (c) Extracted values of V_{th} and μ as a function of V_{CG}. (d) Extracted values of S as a function of V_{CG}. V_{CG}: coplanar-gate voltage.

Both the depletion mode and the enhancement modes can be used as the basic building blocks to construct complementary 2-D IC, which will have less power consumption and more functionality.

We summarized the extracted values of V_{th} and μ in Fig. 4(c). From this figure, V_{th} has a nearly linear dependence from −0.55 to 6.4 V as a function of the top coplanar-gate voltage. Such a dual-gate MoS_2 FET with coplanar gate may have some important applications, such as ion-sensitive sensor FETs (ISFETs) [22]. In general, an ideal ISFET should have good sensor characteristics to the variation of external environment (that is through the voltage potential on the additional dielectric). Here, our device shows a great potential for application as an ISFET based on the following reasons: 1) V_{th} shows a large variation from −0.55 to 6.4 V as a function of the top coplanar-gate voltage, indicating that good sensor characteristics in the surface potential of a coplanar-gate dielectric region can be observed and 2) Compared with the traditional ISFET, our prototype of the dual-gate MoS_2 FET has less process steps. We do not need to fabricate the additional second gate dielectric, which means the device process can be greatly simplified. Based on the V_{th} values and (1), μ can be extracted from the linear region of transfer curves in Fig. 4(a) by using the SiO_2 dielectric capacitance: $C_i = (\varepsilon_o \varepsilon_r / d) = 1.19 \times 10^{-8}$ F/cm^2, where ε_o is the dielectric constant of vacuum, ε_r is the relative dielectric constant of SiO_2 ($\varepsilon_r = 3.9$), and d is the thickness of the SiO_2 dielectric ($d = 290$ nm). The results are shown in Fig. 4(c). The μ value was calculated to be ∼5.4 cm^2/Vs, which was almost independent of different coplanar-gate voltages. We note that the μ value is larger in a dual-gating mode than in a single-gating mode of our device. The possible reason is that it is not true conductivity mobility, but it is the field-effect mobility [23], which increases as charge density increases during dual-gate operation. Compared with the single-gating

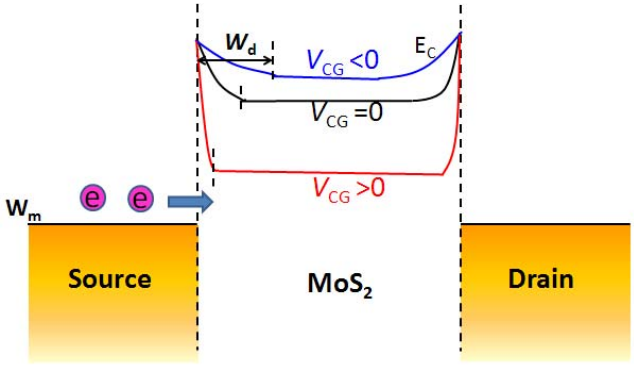

Fig. 5. Schematic energy band diagram of a coplanar dual-gate MoS_2 FET for explaining the V_{th} shift.

mode, a dual-gating mode can provide stronger electric-field coupling between the gate and the channel (that means a larger ON-current) [24]–[26]. Therefore, larger field-effect mobility can be achieved in a dual-gating mode than a single-gating mode. However, compared with the mobility (several hundreds of cm^2/Vs) in conventional Si-based MOSFETs, the mobility in our device is still much smaller (<10 cm^2/Vs). The mobility of MoS_2 transistors can be grossly underestimated due to very high contact resistances associated with Schottky barriers at the source and drain [21]. This requires better source/drain electrode engineering, In addition, further improvement of the drain current in our coplanar-gate MoS_2 devices could be possible with higher quality MoS_2 thin films and use of high-k gate dielectric to get a stronger gate coupling. Furthermore, the subthreshold swing (S) was found to be ~0.5 V/decade with a weak dependence on the different coplanar-gate voltages, as shown in Fig. 4(d), indicating that no additional defects were generated during the continuous coplanar-gate bias [27]. It is also to be noted that, two coplanar-gate electrodes may eliminate any effect due to asymmetry between the coplanar gate and the channel. Unluckily, at present, we have not fabricated the MoS_2 transistor with two coplanar-gate electrodes. In the next work, we shall design two coplanar-gate electrodes into the MoS_2 transistor to examine the effect due to asymmetry in the geometry of the coplanar gate and the channel.

Finally, based on the above results, an energy band diagram similar to the body effect in traditional MOSFET [28] can be proposed to explain the dual-gate modulation in the coplanar-gate MoS_2 FET as shown in Fig. 5. When the coplanar-gate bias (V_{CG}) is zero, the electrons ejecting from source electrode need to overcome high Schottky barriers at the metal-MoS_2 interface (indicated by the black curve in Fig. 5) [21], [29]. More electrons in the MoS_2 channel will be depleted when a negative V_{CG} is applied to the top coplanar gate. Therefore, the depletion region at the metal-MoS_2 interface gets larger, which will make the V_{th} value of dual-gate MoS_2 FET shift toward positive direction (indicated by the blue curve in Fig. 5). However, when a positive V_{CG} is applied, the depletion width will be greatly shortened. Thus, the electrons injected from source electrode have a higher probability to tunnel through this shorter depletion width (indicated by red curve in Fig. 5). V_{th} of the dual-gate MoS_2 FET will shift toward the negative direction accordingly.

IV. Conclusion

In summary, we have successfully fabricated the coplanar-gate multilayer MoS_2 FET without top dielectric. The MoS_2 channel and the coplanar gate are effectively coupled by the bottom-conducting Si substrate. The coplanar-gate MoS_2 FET shows a good performance with a large $I_{ON/OFF}$ of 1.5×10^4, a small S of 0.13 V/decade, and μ of 0.69 cm^2/Vs, respectively. Furthermore, by employing the back-gate in conjunction with the coplanar gate, a dual-gate MoS_2 FET configuration was realized. Such a dual-gate MoS_2 FET has a large V_{th} modulation (−0.55~6.4 V) by changing the coplanar-gate bias from 20 to −15 V, which make the device switch from a typical depletion-mode operation to an enhancement-mode operation. It was found that the μ and S values were ~5.4 cm^2/Vs and 0.5 V/decade, respectively, regardless of different coplanar-gate biases. The coplanar-gate MoS_2 FET and its dual-gate configuration do not require top dielectric engineering, and the deposition of source/drain/coplanar-gate can be shortened to be a single step. Such a coplanar-gate design with its dual-gate operation with a simple fabrication process may represent a significant step toward low-cost 2-D planar nanoelectronics.

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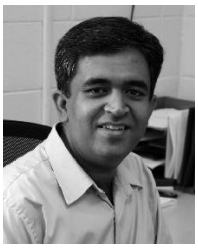

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