A Low-Power Current-Mode Defuzzifier for Fuzzy Logic Controllers

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***Abstract*—In this paper a new current-mode circuit to realize the center-of gravity (COG) defuzzifier is presented. The circuit employs floating-gate MOS (FG-MOS) transistors that operate in weak inversion region. Compared to the other proposed circuit, this circuit features severe reduction of the elements number, low supply voltage (0.7V), low power consumption (<1uW), immunity from body effect and wide input dynamic range (>60dB). Simulation results by Hspice confirm the validity of the proposed design technique and show high performance of the circuit.**

I. INTRODUCTION

Fuzzy systems have drawn a great attention for their capability of translating expert knowledge expressed by linguistic rules into a mathematical frame work [1]. Fuzzy systems can be implemented with software on standard digital processors [2]. However, when real-time operation or low-area and low-power/low-voltage are required, it is suitable to implement them with hardware (fuzzy chips). A fuzzy logic controller consists of four fundamental units: fuzzifier unit, decision-making logic unit, defuzzifier unit and knowledge unit. One hardware realization method for fuzzy logic controller is using digital circuits [3]. However, digital implementation of center-of-gravity (COG) defuzzifier needs digital multiplier and divider circuits which lead to a large chip area and high power consumption [3]. Afterwards, to overcome these shortcomings some analog circuit designs based on current-mode approach have been proposed [4-6]. Current-mode approach gives their design more advantages, such as simple addition/subtraction and low circuit complexity compared with conventional digital and voltage-mode analog signal processing. One attempt is to employ BiCMOS translinear multipliers and dividers for COG defuzzifier implementation [4]. Despite of the advantages, this circuit needs complicated fabrication processes. Following this technique, a current-mode defuzzifier by employing geometric-mean and squarer-divider functions is presented [5, 6]. For design of these functions stacked translinear loops has been employed. The main drawbacks of this proposed design are as follows: firstly, the extra needed functions lead to a large number of transistors and high power consumption; secondly, in this circuit, the MOS transistors are operating in strong inversion, thus employing low-voltage supply restricts dynamic range; and finally, in the circuit of stacked translinear MOSFET loops, the body effect decrease the accuracy [8].

In this paper, a new circuit design to overcome the above problems is presented. In the proposed circuit, which is employed by FG-MOS transistors, circuit complexity is much less than those reported before [2-6]. This circuit is immune to the body effect, because the source of transistors is connected to the substrate. Also due the fact that the transistors are operating in weak inversion, the proposed circuit features low-power, low-voltage and wide dynamic range.

The paper is organized as follows. In section 2 the basic principle of current-mode defuzzifier is discussed. Section 3 explains the proposed circuit design for the COG defuzzifier. Simulation results are presented and discussed in section 4 and concluding remarks are provided in section 5.

II. CURRENT-MODE COG DEFUZZIFER

To implement fuzzy logic controller, Fuzzy sets are mathematically described through membership functions, which return a value between 0 and 1 representing the membership degree of a given variable to the corresponding fuzzy sets. A typical fuzzy processing should be completed with fuzzy inference process that consists of a number of rules. A generic fuzzy rule can be written in the form:

If (a set of conditions are satisfied), **Then** (a set of consequents can be inferred).

In the inference process the degree of truth of the rule premise is evaluated. This value is carried out to the consequent. Fuzzy values produced by a fuzzy inference process are used to produce a crisp value by a COG defuzzifier as follows:

$$COG = \frac{\sum_{i=1}^{N} y_i \mu_{y_i}}{\sum_{i=1}^{N} \mu_{y_i}} \quad (1)$$

where μ_{y_i} is the activation degree of each rule, y_i is the fuzzy label corresponding to the output fuzzy set Y_i and N is the number of rules.

By rearranging the definition of the function in order to hardware implementation of the defuzzifier circuit, each membership degree of the fuzzy set in this work is represented by a continuous current signal within [0nA, 300nA] to indicate the degree of membership belonging to the corresponding fuzzy sets in the universe of discourse. Employing current-mode approach and using (1), the output crisp signal of defuzzifier can be expressed in current-domain as follows:

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$$I_{COG} = \frac{\sum_{i=1}^{N} I_{y_i} I_{\mu_{y_i}}}{\sum_{i=1}^{N} I_{\mu_{y_i}}} \tag{2}$$

where $I_{\mu_{y_i}}$, I_{y_i} and I_{COG} are the current representation of signals μ_{y_i}, y_i and COG, respectively.

By breaking out the weighted summation of the numerator terms of (2), and also using the fact that $\frac{x+y}{z} = \frac{x}{z} + \frac{y}{z}$, it can be rewritten as:

$$I_{COG} = \frac{I_{y_1} I_{\mu_{y1}}}{I_\Sigma} + \frac{I_{y_2} I_{\mu_{y2}}}{I_\Sigma} + \cdots + \frac{I_{y_N} I_{\mu_{yN}}}{I_\Sigma} \tag{3}$$

where $I_\Sigma = \sum_{i=1}^{N} I_{\mu_{y_i}}$.

Fig. 1 shows block diagram of the current-mode COG defuzzifier based on (3). It consists of N multiplier/divider unit, as the fundamental units of the COG defuzzifier, which are connected in parallel form.

III. Proposed Circuit Design

A. Multiplier/Divider

A good choice for circuit design of multiplier/divider is using FG-MOS transistors that operate in weak inversion [9]. A FG-MOS transistor has an isolated gate that capacitively coupled to the input gates. Fig. 2 shows the symbol diagram and equivalent circuit of the transistor with 2 input voltages. The drain current of a N-type FG-MOS transistor, with 2 input gates, in weak inversion is given by [10]:

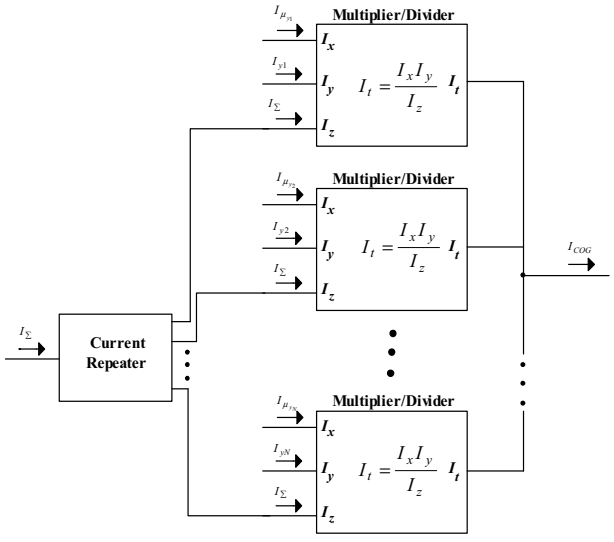

Figure 1. Block diagram of the current-mode COG defuzzifer

$$I_d = I_s \exp\left(\frac{w_1 V_1 + w_2 V_2}{n U_T}\right) \tag{4}$$

where U_T stands for the thermal potential, I_s is a device dependent coefficient, n represents the subthreshold slope, V_i is the i-th input gate voltage $(i \in \{1,2\})$ and w_i is the i-th input capacitance ratio defined as:

$$w_i = \frac{C_i}{C_t} \tag{5}$$

in which C_i is the input capacitance between the floating gate and the i-th input gate and C_t is the sum of these input capacitances.

Fig. 3 shows the circuit of a one-quadrant multiplier/divider that consists of four FG-MOSs operating in weak inversion [9]. Using (4), the I-V relationships for transistors M1, M2, M3 and M4 are expressed as follows:

$$I_1 = I_s \exp\left(\frac{w_{11} V_1 + w_{12} V_3}{n U_T}\right) \tag{6}$$

$$I_2 = I_s \exp\left(\frac{w_{21} V_2 + w_{22} V_3}{n U_T}\right) \tag{7}$$

$$I_3 = I_s \exp\left(\frac{w_{31} V_3 + w_{32} V_3}{n U_T}\right) \tag{8}$$

$$I_4 = I_s \exp\left(\frac{w_{41} V_1 + w_{42} V_2}{n U_T}\right) \tag{9}$$

It is assumed that the areas of the floating gates for all transistors are twice of the areas of the external gates, i.e., $w_{11} = w_{12} = w_{21} = w_{22} = w_{31} = w_{32} = w_{41} = w_{42} = \frac{1}{2}$. In such case, it can be shown multiplication (6) by (7) and (8) by (9) and then comparing the results, it is obtained as follows:

$$I_1 I_2 = I_3 I_4 \quad \rightarrow \quad I_4 = \frac{I_1 I_2}{I_3}. \tag{10}$$

Therefore, a one-quadrant multiplier/divider circuit is obtained by taking a copy of I_4 as the output, and copies of I_1, I_2 and I_3 as the inputs.

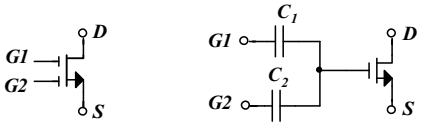

Figure 2. Symbol diagram (left) and equavalent circuit of FG-MOS (right)

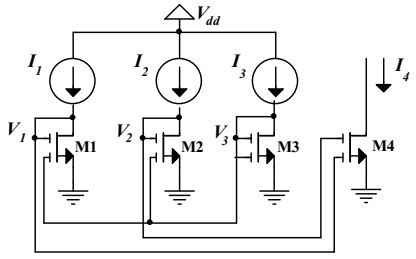

Figure 3. A FG-MOS based one-quadrant multiplier/divider[9]

As Fig. 3 shows, the number of components in the proposed circuit is much less than those reported before [2-6]. Also the source of transistors is connected to the substrate, so the body effect is eliminated. In addition, as the transistors are operating in weak inversion, these circuits can work in low-power, low-voltage and wide dynamic range. This Figure reveals that, the minimum supply voltage of the circuit is one V_{gs} plus one V_{ds}.

B. Case Study: One-Dimensional Defuzzifier

In this subsection, the proposed multiplier/divider is employed for circuit design of a one-dimensional (one input control signal and one output signal) current-mode defuzzifier. In such case, the input signal should fire two rules each time [5]. The membership functions associated with these two fired rules are adjacent and complementary to each other. By this assumption, using (2), the output crisp signal of COG defuzzifier can be expressed as follows:

$$I_{COG} = \frac{I_{y_1} I_{\mu_{y1}}}{I_{\Sigma}} + \frac{I_{y_2} I_{\mu_{y2}}}{I_{\Sigma}} . \qquad (11)$$

Fig. 4 shows the complete circuit of the proposed defuzzifier, which consists of two multiplier/divider unit. In this circuit, transistors M1-M4 form first multiplier/divider unit, transistors M3, M5-M7 are employed for second multiplier/divider unit and remaining transistors are employed for injecting the proper currents into these units. It should be pointed out that transistor M3 is common element for both multiplier/divider units and are merged, which it results reduction of elements number.

IV. SIMULATION RESULTS

The proposed circuits of Fig. 3 and Fig. 4 were simulated using Hspice with 0.18um TSMC CMOS process parameters. The supply voltage of 0.7V was employed. The aspect ratios of the N-type and P-type transistors were chosen 10um/10um and 20um/10um, respectively. For FG-MOS transistors the model of reference [11] is used. To verify the function of the multiplier/divider circuit of Fig. 3, the triangle membership functions with amplitude of 400nA is applied for the input current I_1. Fig. 5 shows the output signal I_4 versus input response I_1, where the input current I_2 was stepped from 30nA to 300nA in 30nA steps and also the input current I_3 was set to 300nA (plot down to up). The power consumption of this circuit is less than 200nW and the maximum absolute error is within 0.7%.

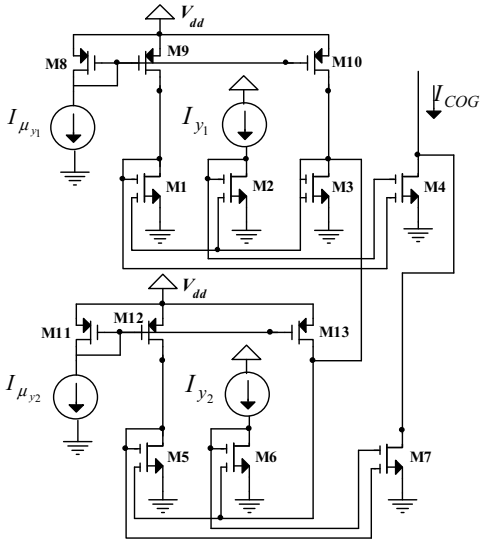

Figure 4. The complete circuit diagram of the proposed current-mode COG defuzzifer

In order to confirm the accuracy of the proposed defuzzifier, the circuit of Fig. 4 was simulated. The simulation results are shown in Fig. 6. In this simulation, input signals are applied the triangle membership function, which are frequently used in fuzzy control system, and $y_i \in [0, 1]$ are mapped to $I_{\mu_{y_i}} \in$ [0nA, 300nA]. Also, the value of I_{y_1} and I_{y_2} were set to 400nA and 200nA, respectively. The results show that the output of the proposed circuit is almost consistent with the ideal case. Therefore, this circuit can perform the function of COG defuzzifier. Simulation results showed the power consumption of defuzzifier circuit is less than 1uW and the maximum absolute error is within 1.3%. Also, the dynamic range is more than 60dB. A comparison was made with formerly reported one-dimensional defuzzifier circuits. Table I summarizes this comparison by showing some important parameters of the circuits.

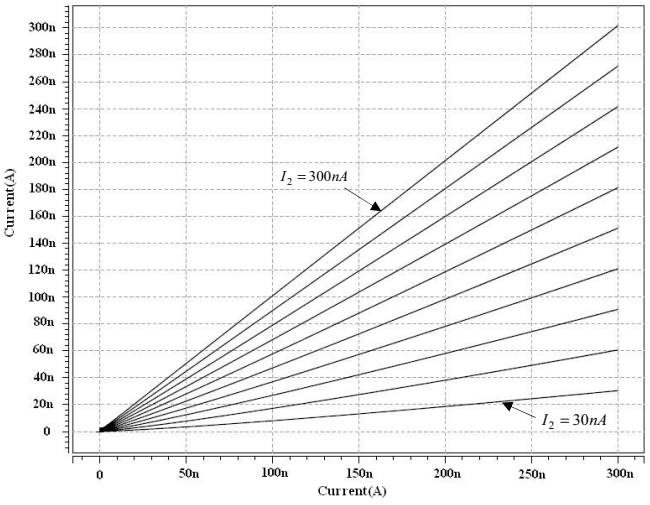

Figure 5. Output current I_4 versus input current I_1 for multiplier/divider circuit of Fig. 3 at different values of input current I_2

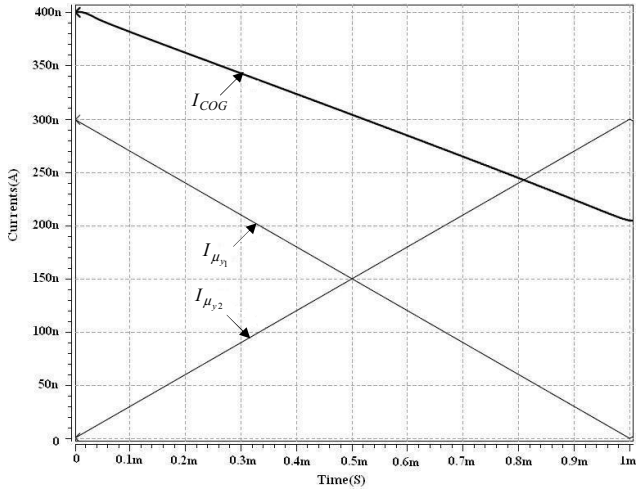

Figure 6. Output current (bolded) and input currents for defuzzifier circuit of Fig. 4

TABLE I. A COMPARIISION BETWEEN DIFFERENT ONE-DIMENSIONAL DEFUZZIFIER

Parameter	Ref. [5]	Ref. [6]	Ref. [7]	This Work
Technology	0.8u	0.35u	0.35u	0.18u
Supply Voltage	3.3V	3.3V	3.3V	0.7V
Power Consump.	>1mW	Expected >1mW	>1mW	<1uW
Transistor Count	>70	>70	>31	13
Input Range	Expected <24dB	Expected <24dB	Expected <26dB	>60dB
Body Effect	Yes	Yes	Yes	No

V. CONCLUSION

A new COG defuzzifier circuit design based on multiplier/divider is presented. The circuit employs FG-MOS transistors that operate in weak inversion region, is with low circuit complexity, is immune from body effect and works at low-voltage/low-power. Simulation results of the circuit show that the technique is promising and can be used in the fuzzy logic controller integrated circuits.

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