A CMOS Implementation of Current-Mode Min-Max Circuits and A Sample Fuzzy Application

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***Abstract*— A new design of CMOS Min-Max circuits in current-mode is presented. These kinds of circuits have a growing number of fuzzy applications in fuzzy logic controllers. As a sample fuzzy application, Membership Function Generator (MFG) based on Min circuit, is presented. The proposed circuits have wide input and output dynamic range. A 3.3 V power supply has been applied and simulation results are presented in 0.35 μm CMOS process.**

I. INTRODUCTION

In last decade a growing number of fuzzy applications in hardware level implementations, such as fuzzy logic controllers [1]-[5] has been proposed. In these kinds of application, basic operations and their implementations play a great role. Any improvement in circuit level realization of these basic operations, can lead us to have an efficient circuitry for such an application. There are two different perspectives in implementation of this operation: Digital and Analog implementations [1]. In digital approaches low cost, fast and easy design flow and accuracy are some of important advantages. On the other hand the output of implementation for a simple basic operation can be a huge VLSI circuit with area and power consumption problems. In Analog perspective, basic operations can be implemented with smaller circuits but accuracy and range of functionality are serious items, which should be considered carefully.

Among basic operations, Min-Max operations in circuit level are used in many hardware implementations of fuzzy logic applications. In fuzzy processors [6] and fuzzy logic controllers [7], [8] these basic operations play a crucial role. On the other hand, Membership Function Generator (MFG) circuits, which are constructed based on basic operations, are used to calculate fuzzy membership value of input variable. Fuzzy circuit designers are interested in designing efficient and accurate MFGs to use in fuzzy logic applications [9], [10]. In MFGs the input-output mode can be voltage-voltage [4], voltage-current [11] or current-current [2], [9], [12]. Our proposed Min-Max circuits which are built using current mirrors, have a wide input and output dynamic range with acceptable accuracy in their functionality rang.

To show the performance of these circuits, an implementation of MFG circuit in current-current input-output mode is presented. Comparing other circuitry for this kind of circuits in different fuzzy application, proposed circuit has better input and output variation range and slopes of each side can be changed independently to form trapezoidal and triangular Membership Functions.

II. CURRENT MIRRORS

The basic element of our proposed Min-Max circuits is Current Mirror (CM). There are different implementations for CMs for example: Simple Current Mirror (SCM), Cascode Current Mirror (CCM) and Wilson Current Mirror (WCM). These three structures are shown in Fig. 1. The important difference between SCM and the other two ones is accuracy and minimum voltage in headroom. To gain a better view, we compare SCM and CCM in these two facts but the principles are the same for WCM also. In SCM, since the gate-source voltage of M_1 and M_2 are equal, the current of two transistors can be equal but because of channel length modulation (λ) and since M_1 and M_2 might have unequal drain-source voltage; output current does not accurately track I_{REF}. We can write:

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_T)^2 (1 + \lambda V_{DS1}) \quad (1)$$

$$I_{OUT} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_T)^2 (1 + \lambda V_{DS2}) \quad (2)$$

Dividing (2) by (1):

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} \quad (3)$$

In this structure the minimum voltage at node X can be one overdrive voltage ($\Delta V = V_{GS} - V_{TN}$). According to (3) to have accurate current mirroring we must have equal

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drain-source voltage for M_1 and M_2. In CCM structure, M_3, M_4 cause to have equal voltages at X and Y assuming proper transistor sizing $((W/L)_4/(W/L)_3=(W/L)_1/(W/L)_2)$ [13]. On the other hand minimum voltage at node Z is two overdrive voltages plus one threshold voltage [13], [14] then it can be concluded that this structure consumes more voltage in headroom but it is more accurate than SCM.

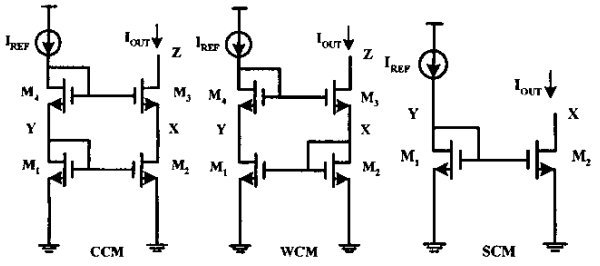

Fig. 1. CCM, WCM and SCM Structures

According to these considerations we choose CCM to use in our Min-Max circuits. With this choice, voltage swing at output is limited and therefore functionality range for whole circuit is decreased but more accuracy is achieved.

III. PROPOSED MIN-MAX CIRCUITS

The principle of our proposed Min-Max circuits comes from following expressions:

$$Min(a,b)=\frac{a+b}{2}-\frac{|a-b|}{2} \tag{4}$$

$$Max(a,b)=\frac{a+b}{2}+\frac{|a-b|}{2} \tag{5}$$

If we assume $a>b$ then the second terms of right statement in expressions above will be equal to $(a-b)/2$ and (4) and (5) reflect b and a respectively which are minimum and maximum values between them. Otherwise the absolute value for $a-b$ will be equal to $b-a$ and (4) and (5) will reflect a and b respectively.

To realize (4) and (5) in circuit level, circuits shown in Fig. 2. and Fig. 3. are proposed. In Fig. 2 the CCM consisting of M_1-M_4 is responsible for producing the term of $(I_1+I_2)/2$. The size of M_1 and M_2 are twice as much as the size of M_3 and M_4. Two similar CCM structure consisting of M_5-M_8 and M_9-M_{12} are producing the second term at the right side of expressions (4) and (5). When $I_1>I_2$ in the upper CCM all of four transistors go to cut-off region. In this case CCM consisting of M_9-M_{12} sinks a current equal to absolute value of $(I_1-I_2)/2$ from M_{13} and M_{14}. Otherwise the other CCM will have the responsibility to conduct. PMOS CCM only mirror the same current to output node. It means the size for all of transistors in this CCM (M_{13}-M_{16}) can be equal. In Fig. 3 the same principle has been used but M_{15} and M_{16} are eliminated to have sum operation between currents at output node. In this case the output can be equal to the maximum value of I_1 and I_2. In these circuits using SCM can increase the input and output current range and also can decrease the active area of whole circuit but in this case the accuracy of circuit will be decreased. As we discussed, in Fig. 2 the currents can be increased until the voltage of output node does not come to less than two overdrive voltage plus one threshold voltage ($2\Delta V + V_{TN}$) and for upper band of voltage at output node it is obvious that M_{15} and M_{16} need at least $2\Delta V + V_{TP}$ to be in saturate region. To summarize our discussion about voltage limitation at output node of circuit shown in Fig.2 neglecting body effect and assuming equal threshold voltage for all NMOS transistors (V_{TN}) and also for all PMOS transistors (V_{TP}), we can write:

$$2\Delta V_1+V_{TN}< V_{Out}< V_{dd}-[2\Delta V_2+V_{TP}] \tag{6}$$

As it was mentioned, in (6) $\Delta V= V_{GS} - V_T$ and V_{GS} is equal for all of four transistors in CCM structure. From (6) and by considering general current equation for CMOS transistors (expressed in (1) and (2)) the limitation for input and output current ranges can be achieved. The principle is the same for Max Circuit shown in Fig. 3.

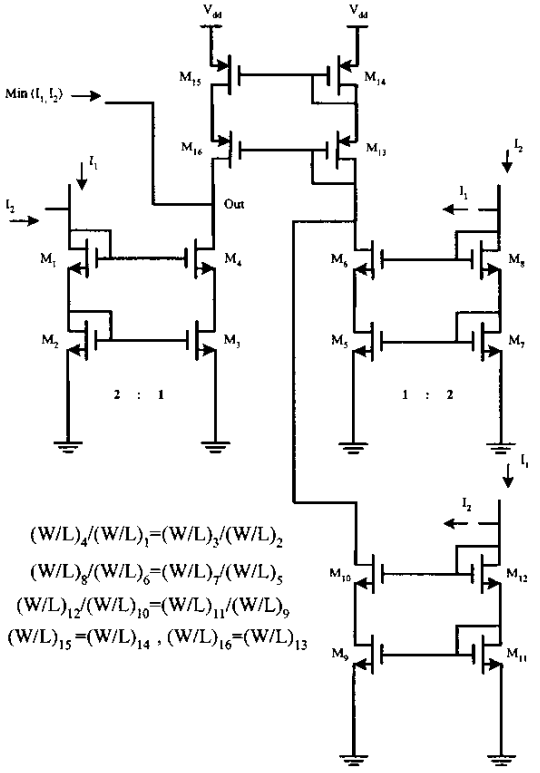

Fig. 2. Proposed Min Circuit

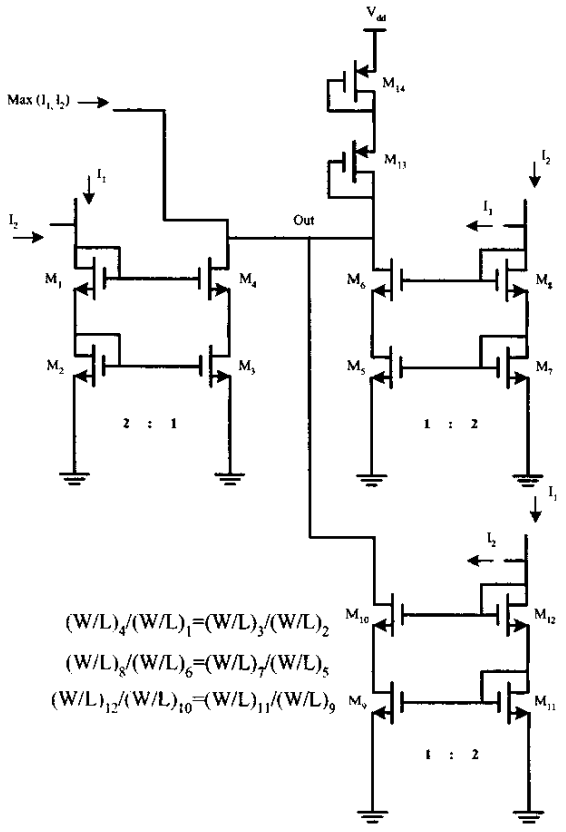

Fig. 3. Proposed Max Circuit

IV. MEMBERSHIP FUNCTION GENERATOR

In fuzzy applications Membership Functions (MFs) are used for determination of fuzzy membership value for input variable. Each input should be translated to a specified fuzzy membership value. Typical MFs are defined in trapezoidal or triangular approximations when sketching output versus input variable. In current-current mode input and output values are defined as currents. In this case MF can be specified by five different values. These values are shown in Fig. 4. By using these values, position and shape of MF are specified. I_L and I_H are defined as lowest and highest input currents which has nonzero fuzzy membership values. I_{max} represents maximum membership value and K_1 and K_2 are slope values of each side. To form a triangular MF these five values should be defined in such a way that two slops can meet each other before reaching to I_{max}. We will call "left slope" to the slope beginning at I_L and "right slope" to the slope ending at I_H.

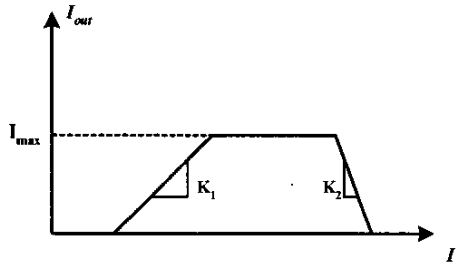

Fig. 4. A Trapezoidal MF

As mentioned, to show the performance of our proposed Min-Max circuits, a CMOS implementation of MFG in current mode based on Min circuit is presented. In this MFG, algorithm in order to build a typical MF is as following.

First of all, I_{in} is compared with I_L and I_H. If $I_{in} < I_L$ or $I_{in} > I_H$ the value of output current will be zero. Otherwise two currents according to right and left slopes are produced. Mathematically these two currents are $K_1.(I_{in}-I_L)$ and $K_2.(I_H-I_{in})$. Then these currents are compared with I_{max}. The minimum value among these currents will be the output current. Therefore proposed MFG needs a circuit to generate currents according to right and left slopes and also three Min circuits to compare generated currents with I_{max}.

A. Slope Definition

In order to generate currents according to K_1, K_2 the circuits shown in Fig. 5 is used. These circuits are consisting of two CCMs, which multiply incoming current by value of the slopes. As we mentioned, if I_{in} does not satisfy $I_L < I_{in} < I_H$ the output current will be zero. In this case, in the circuits shown in Fig. 5, all transistors will be entered in cut-off region and no current will be reflected to I_{Left} and I_{Right}. This means there will be a comparison between I_{max} and 0, which obviously will have the result of zero current at the output of MFG circuit.

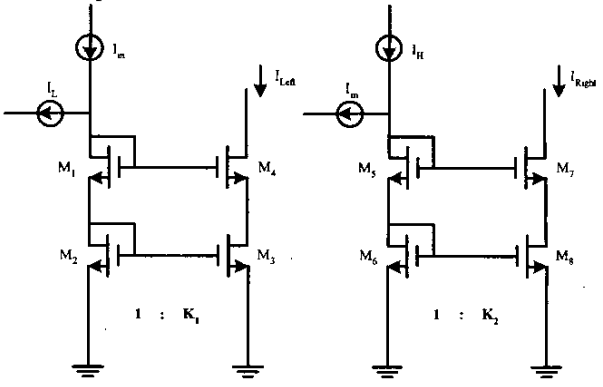

Fig. 5. Circuits for Generating Currents According to K_1 and K_2

In Fig. 5 the values of generated currents will be:

$$I_{Left} = \begin{cases} K_1(I_{in} - I_L) & I_{in} > I_L \\ 0 & I_{in} \le I_L \end{cases} \quad (7)$$

$$I_{Right} = \begin{cases} K_2(I_H - I_{in}) & I_{in} < I_H \\ 0 & I_{in} \ge I_H \end{cases} \quad (8)$$

B. Realization of MFG Using Min Circuits

In the last step of implementation of MFG, the generated currents by slope defining circuits (I_{Right}, I_{Left}) should be compared with I_{max} which is one of the characteristics of MF. To do this, three Min circuits are required in order to determine the minimum value among these three currents. The proposed circuit to construct our current mode MFG is shown in Fig. 6.

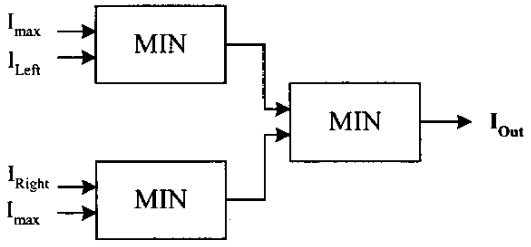

Fig. 6. Proposed MFG Structure

In circuitry of MFG in order to transfer current to different parts of circuit CCM structure has been used as discussed in previous sections.

V. Simulation Results

To check the functionality of Min-Max and MFG circuits different simulations have been performed using Hspice simulator and 0.35μm CMOS process transistor models. These simulations have been done in two steps. First of all the circuits shown in Fig. 2 and 3 have been simulated and then structure shown in Fig. 6 using three Min circuits and other related circuits shown in Fig. 5 have been checked by proper simulations.

A. Min-Max Circuits Simulation Results

The proposed Min circuit shown in Fig. 2, has been simulated using Hspice simulator. For this circuit two different simulation results are shown in Fig. 7 and 8. In Fig. 7 a sinusoidal current with 200μA dc level and 50μA amplitude has been compared with a dc constant 230μA current. In this figure, in the lower window two input currents of this circuit are shown and in the upper window resulted output current from this circuit is shown. The sinusoidal current is limited by constant 230μA dc current. In Fig. 8 a pulse shape current has been compared with a sinusoidal current. The resulted minimum current in the output of the circuit has been shown in the upper window.

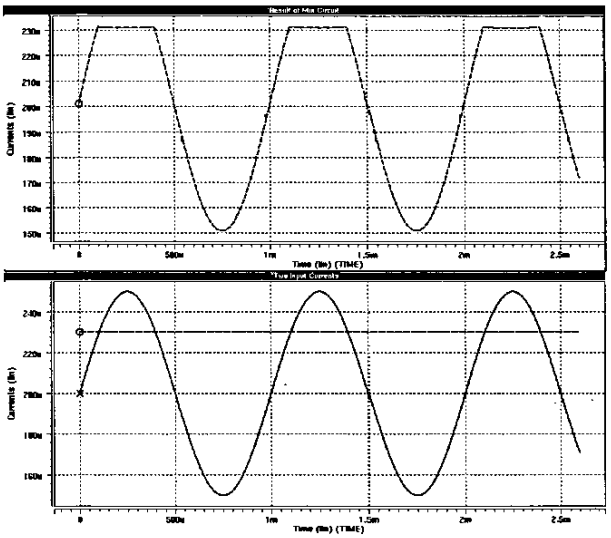

Fig. 7. Simulation Result of Min Circuit

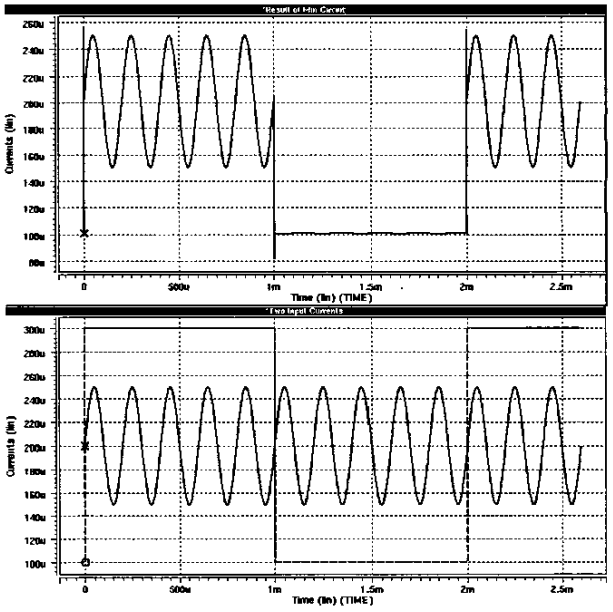

Fig. 8. Another Simulation for Min Circuit

In Fig. 9 the simulation result related to Max circuit is presented. In this simulation circuit shown in Fig. 3 has been simulated using a sinusoidal current with 290μA dc

level and 40μA amplitude and a dc constant 280μA current. In this figure the lower window shows input currents and in the upper one, resulted current in the output of this circuit has been shown. In the resulted current sinusoidal part cannot be less than 280μA.

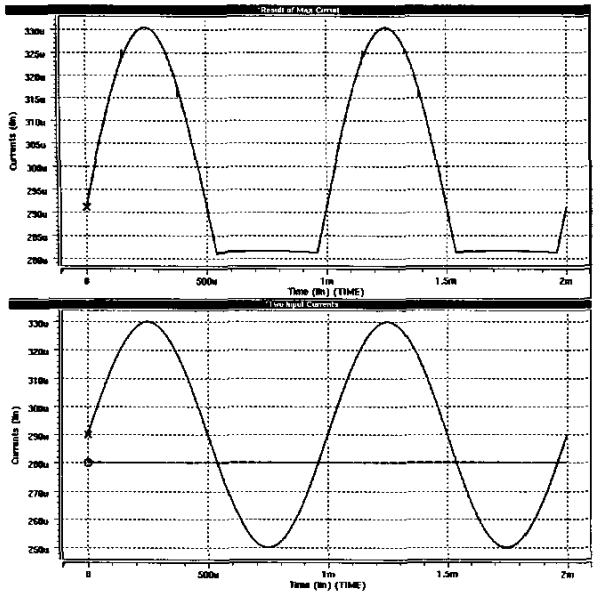

Fig. 9. Simulation Result for Max Circuit

In these kinds of circuits the difference between the ideal expected output current after comparison and the actual resulted current in circuit level simulation, can be defined as error and determines accuracy of circuit. From different simulations it can be concluded that by proper transistor sizing, in a 150μA input current range proposed Min-Max circuits can be operate with less than 1% error in defining output current.

B. MFG Circuit Simulation Results and Comparison

In the second step in order to check the functionality and the performance of MFG circuit, which has been built using proposed Min circuit, structure of Fig. 6 has been simulated. As mentioned, I_{Left} and I_{Right} are produced using circuits shown in Fig. 5 and current transfer is done using CCM structure. To form desired MFs, according to definition of MF, after applying five quantities discussed in section IV, a varying input current (like sinusoidal waveform) has been applied and output current of MFG circuit has been formed versus its input current. The simulation results of this circuit are shown in Fig. 10 and 11. In these simulations two different MF is produced using proposed scheme. In Fig. 10 a trapezoidal MF has been shown. In this MF, I_L=110μA I_H=240μA and I_{max}= 85μA and two slopes has been defined unequal. In Fig. 11 by decreasing left side slope for trapezoidal MF a triangular one is obtained.

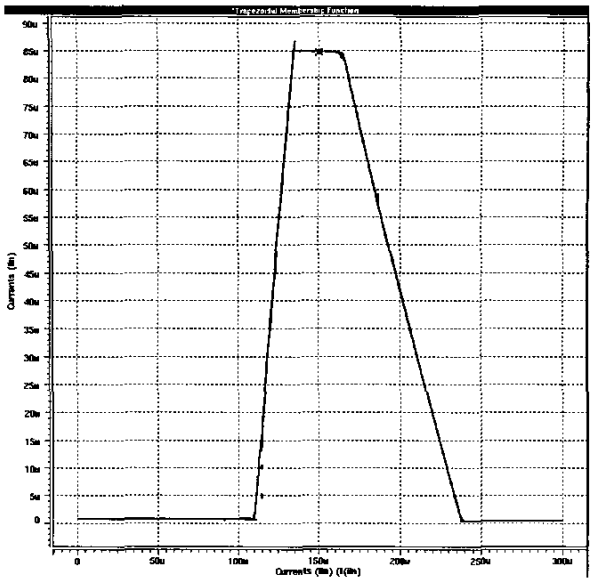

Fig. 10. A Trapezoidal MF I_L=110μA, I_H=240μA and I_{max}= 85μA

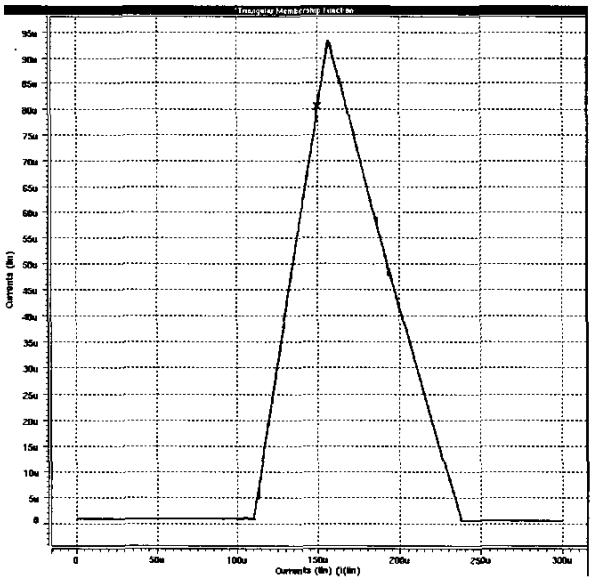

Fig. 11. A Triangular MF I_L=110 μ A, I_H=240 μ A

The proposed MFG circuit has a 130μA input current range and 100μA output current range. The slopes of both sides in MF can be defined independently and can be unequal. Comparing previous MFG circuits in current-mode, input and output ranges for this MFG circuit are quite wide. To have a comparison, input and output ranges

for three different previous designs have been compared with our proposed MFG circuit in Table I. In these three designs, proposed MFG circuits are in the current-current input-output mode.

TABLE I

A Comparison Among Previous Works & Proposed MFG Circuit

Reference No.	Input Range	Output Range
[2]	50 μA	20 μA
[9]	100 μA	100 μA
[12]	50 μA	10 μA
Proposed Design	130 μA	100 μA

VI. CONCLUSIONS

A new implementation for Min-Max circuits in CMOS process has been presented. These circuits are based on current mirrors. According to results obtained from simulations in 0.35μm CMOS process, these circuits can operate in a 150μA input current range with less than 1% error. As a fuzzy application a Membership Function Generator circuit based on these basic operations has been presented. This circuit can produce different trapezoidal and triangular MFs in a 130μA input and 100μA output range. These ranges are quite wide comparing previous works.

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