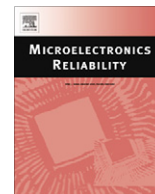




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A partial-SOI LDMOSFET with triangular buried-oxide for breakdown voltage improvement

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ABSTRACT

In this paper, a near-triangular buried-oxide partial silicon-on-insulator (TB-PSOI) lateral double-diffused MOS field-effect transistor is proposed. The electric field and electrostatic potential in this structure are modified by the gradual buried-oxide thickness increase. The modification includes the addition of a new peak in the electric field in comparison to that of the conventional PSOI. To assess the efficiency of the proposed structure, its breakdown voltage is compared with that of conventional PSOI using two-dimensional simulations. A comparative study is performed in terms of silicon-film and buried-oxide layer thicknesses, drift region and buried-oxide layer lengths, and drift region doping concentrations. The study shows that under the same drain current, the breakdown voltage of TB-PSOI is nearly two times higher than its PSOI counterpart (108% improvement). Simulation results show that the three-stepped oxide layer closely follows the TB-PSOI structure with a breakdown voltage improvement of 96% compared to that of the PSOI structure.

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1. Introduction

In recent years, lateral double-diffused MOS field-effect transistors (LDMOSFETs) have become the preferred devices for monolithic high-voltage and smart power applications [1,2]. The advantages of these devices over traditional vertical double-diffused MOS field-effect transistors (VDMOSFETs) are reduced fabrication steps, multiple output capability on the same chip, and compatibility with advanced VLSI technologies [3]. LDMOSFETs with VLSI processes make the prospect of intelligent power ICs a reality. For improving the performance of LDMOSFETs, various structures have been proposed [4–6]. The reduced surface field (RESURF) structure is a suitable solution when the tradeoff between on-resistance and breakdown voltage is considered [7–10].

Silicon-on-insulator (SOI) provides a distinct advantage over the traditional junction isolation by further increasing the breakdown voltage and is of great interest for the fabrication of high-voltage lateral devices [11]. Unlike their bulk silicon device counterparts, SOI-based structures present thermal robustness since the parasitic bipolar turn-on in these devices is suppressed and threshold voltage drift is hindered [12]. The buried-oxide in SOI structure provides improved isolation between adjacent circuits [13], which is attractive for the suppression of substrate cross talk in mixed signal circuit applications with integrated power devices. Main drawbacks of the SOI-based structures that have limited their

application in high-voltage ICs are self-heating effects created by the oxide layer acting as a heat flow barrier to the substrate [14], and floating body effects in partial-depleted SOI devices. The floating body effect leads to a kink in the I – V characteristics and causes distortion and ultimately low power efficiency [15]. In switching applications, self-heating effects limit the operation of SOI power devices and may cause short circuit [14]. To alleviate the self-heating effects, partial-SOI (PSOI) technology where a silicon window is created to reduce the self-heating effect, has been employed [16,17].

To further increase the breakdown voltage, several structures such as linearly graded doping profile, composite structures, double-sided trenches on the buried-oxide layer, variable- k dielectric buried layer, and partially SOI LDMOSFET have been proposed [18–25]. Additionally, step drift and two-stage drift techniques are introduced to enhance the hot-carrier immunity in LDMOSFET devices [26,27]. Lastly, a stacked lightly doped drain (LDD) RF LDMOSFET that improves current drive, cutoff frequency and transconductance performance has been reported [28].

In this paper, a new device structure based on a near-triangular buried-oxide and a two-stage drift region is proposed. This near triangular buried-oxide PSOI (TB-PSOI) structure allows significant improvement in the breakdown voltage over its PSOI counterpart. The rest of the paper is organized as follows. In Section 2, practical fabrication steps of the proposed device structure are discussed while the device structure and simulation parameters are described in Section 3. The results for the electric field and potential distributions along with the dependence of the breakdown voltage

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on different physical parameters of the device are discussed in Section 4. Finally, Section 5 concludes the paper.

2. Proposed technology

The schematic cross-sectional view of the proposed PSOI structure is shown in Fig. 1 which shows a triangular buried-oxide. Unless a gray-scale ion implantation technology is used, the triangular buried-oxide structure cannot be realized. To make the device fabrication possible, the triangular buried-oxide layer is approximated by stepped buried-oxide layers. To fabricate the proposed structure, we may use either an SOI or a bulk wafer. First, the area devoted to the CMOS part of the power IC is masked. In the case of SOI wafer, the top silicon and buried-oxide areas are also etched out for the regions which are considered for fabricating the LDMOSFET devices. Next, an epi-layer with a proper doping ($1.8 \times 10^{16} \text{ cm}^{-3}$) is re-grown and then similar to the SIMOX technology, a three-step oxygen implantation with identical doses but different implantation energies is performed. Prior to each implantation step a mask layer that defines the implantation region is patterned. To create a near triangular buried-oxide layer, the deepest implantation region associated with the highest implantation energy is performed within the smallest pattern. The next implantation with slightly smaller energy (shallower implantation than the first one) is done within a larger pattern that includes the first pattern. A third oxygen implantation is done in yet a larger area with the smallest implantation energy (shallowest implantation). After annealing the wafer at elevated temperatures, the oxygen and Si atoms within these regions form SiO_2 bonds in a three-stepped buried-oxide structure. Since the thickness of the crystalline silicon layer above the oxide is not sufficient (50 nm), an epitaxial layer of silicon (450 nm) is grown on top of the silicon thin-film by chemical vapor deposition (CVD) epitaxy (similar to SIMOX process [29]). The dose and energies of the oxygen implants for the required oxide thickness may be obtained from [30]. The oxygen doses for all the three oxygen implantation steps turned out to be $2.1 \times 10^{18} \text{ cm}^{-2}$ while the implant energies were 495, 280, and 100 keV, respectively.

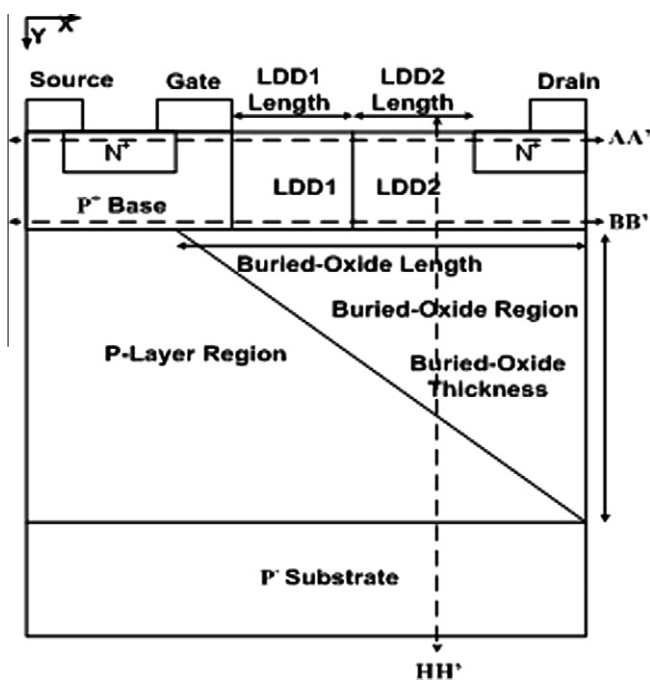


Fig. 1. Cross section of TB-PSOI structure.

Following the approach taken in [28], to have more control over the breakdown voltage and more design parameter flexibility, the drift region in our design is separated into two parts with slightly different doping concentration denoted by LDD1 and LDD2 (see Fig. 1). To have a rather uniform doping profile, we have used two ion implantation steps for each LDD region. To simulate the fabrication process of the device, the Synopsys process simulator tool (Sentaurus Process) [31] was used. The snapshots of the oxide and doping concentration distributions of the structure are shown in Fig. 2.

The breakdown voltage of the structure with three stepped buried-oxide PSOI structure is about 6% lower than that of an ideal TB-PSOI. In the cases of structures with two, four, and five steps, the breakdown voltages are about 9%, 5%, and 4% lower than that of the ideal TB-PSOI, respectively. As the simulation results reveal, there is not much difference between the three to five step oxide layer processes suggesting that using the three-stepped approximation instead of the ideal TB-PSOI provides satisfactory performance. For the rest of the paper, stepped PSOI corresponds to three-stepped PSOI.

3. Device structure and simulation parameters

Due to better carrier confinement, the conventional SOI structure, in which the length of buried-oxide layer extends from the right end of drain to the left end of source, has a larger drain current than the bulk structure. This structure, however, suffers from the self-heating problem. The problem may be alleviated by using partial SOI (PSOI) structure at price of lowering the drain current. Our simulations show that in order to improve the breakdown voltage in PSOI, one should increase (decrease) the thickness of the buried-oxide at the drain (source) side. Therefore, one may consider using a triangular shaped buried oxide. The increase in the breakdown voltage originates from adding a new peak in the horizontal electric field. The simulations of a PSOI structure show that the longer is the silicon window, the smaller is the increase in the drain current compared to that of the bulk structure. Therefore, one can determine the proper length for the silicon window in PSOI based on the drain current. It should be noted that the thermal aspects (heat removal) also play an important role in determining the length of the silicon window, and hence, the window length should be determined based on a trade-off between the drain current and heat removal capabilities of the structure. In this paper, however, our focus is not on the thermal aspects and window length optimization, and therefore, we determined the window length merely based on the drain current.

For the case of triangular buried-oxide structure, if the buried-oxide layer is extended from the right end of the source contact to the right end of the drain contact, the drain current is reduced by about 7% compared to the case where the triangular buried-oxide layer extends to the left end of the source contact (oxide layer is extended under the source contact). Similarly, for the case of rectangular buried-oxide structure, the drain current is reduced by about 6% when the buried-oxide layer does not exist under the source region. Additionally compared to the case where the oxide layer is extended under the source contact, when the buried-oxide layer starts from the right end of the gate, the current is reduced by about 22% (10%) in the case of a triangular (rectangular) structure. Therefore, to minimize the drain current reduction while maximizing the breakdown voltage, in this work, it is assumed that the buried-oxide layer extends from the right end of the drain to the right end of the source. While this leads to slightly lower drain current of the PSOI structure compared to that of the SOI structure as discussed above, the self-heating problem may reduce. Note that in the partially SOI LDMOSFET with two-stepped buried-oxide layer

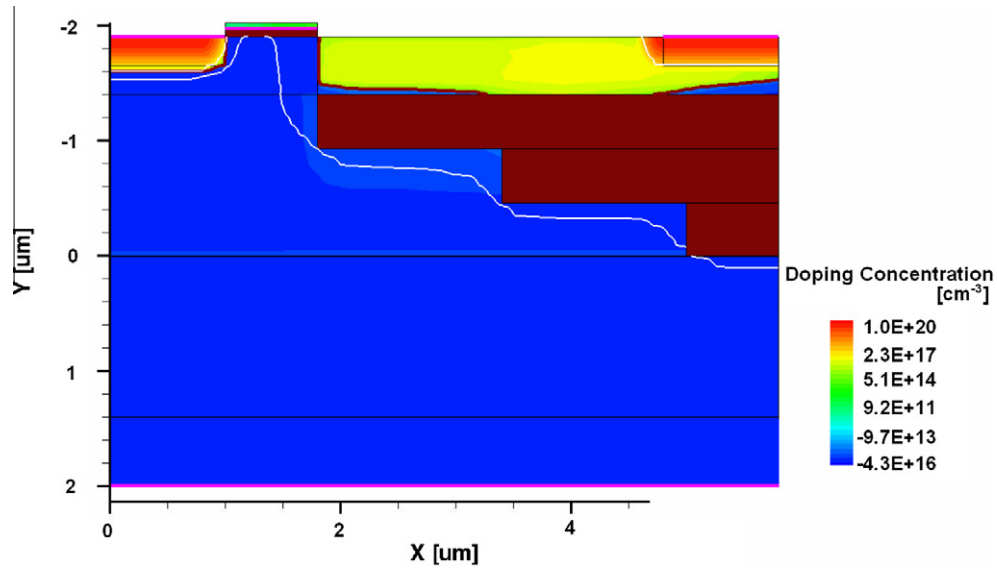


Fig. 2. The snapshot of the oxide and doping concentration distributions of the stepped PSOI obtained using the process simulator.

proposed in [3], the stepped buried-oxide layer covered only part of a single long drift region (device not suitable for high frequency). While the breakdown voltage of this transistor is increased, the drain current drops significantly in comparison to the SOI structure. In our proposed structure, on the other hand, a larger length for the buried-oxide is assumed in order to increase the breakdown voltage while keeping the drain current relatively unchanged. Additionally to be able to make fair comparison, equal buried-oxide volumes for TB-PSOI and conventional PSOI structures are used. In other words, the buried-oxide thickness of TB-PSOI at the drain bottom is two times greater than that of the conventional PSOI.

The structure is studied using the Synopsys device simulator tool (Sentaurus Device) [32]. The device parameters used in this work are given in Table 1. It should be noted that the models used in our simulations include doping dependence mobility, high field saturation effects, vertical electric field dependence model (Enormal model), and carrier–carrier scattering (Brooks Herring model) for the mobility and Shockley–Read–Hall model, Auger, and Avalanche (Van Overstraeten model) recombination models. Furthermore, an effective intrinsic density model (Slotboom model) is used. Breakdown voltage is determined from silicon critical electric field of 3×10^5 V/cm.

Table 1
Device dimensions and doping concentrations for the structure of Fig. 1.

$N_{P-layer}$	$1.8 \times 10^{16} \text{ cm}^{-3}$
$N_{substrate}$	10^{16} cm^{-3}
$N_{channel}$	$3 \times 10^{16} \text{ cm}^{-3}$
N_{LDD1}	$1.65 \times 10^{16} \text{ cm}^{-3}$
N_{LDD2}	$2.9 \times 10^{16} \text{ cm}^{-3}$
$L_{channel}$	0.8 μm
$L_{source/drain}$	1.0 μm
L_{LDD1}	1.5 μm
L_{LDD2}	1.5 μm
L_{BOX}	4.8 μm
$t_{source/drain}$	0.25 μm
t_{Si}	0.5 μm
t_{BOX}	1.4 μm

4. Results and discussion

In this section, first, the results for the electric field and potential distributions for the TB-PSOI, stepped PSOI, and PSOI structures are presented. Then, the effects of varying dimensions of the device as well as the doping concentrations of the drift region on the performance of the device are studied.

4.1. Electric field, potential, and temperature distributions

The applied potential is equal to the area underneath the electric field curve. To enhance the breakdown voltage, the area under the electric field before its maximum reaches the critical field should be increased. Fig. 3 shows the electric fields and electrostatic potentials of PSOI and TB-PSOI at the breakdown voltage of PSOI. As the figure indicates, the electric field and electrostatic potential distributions for TB-PSOI are better than those of PSOI, and therefore, we expect that the breakdown voltage of the proposed structure becomes larger than that of PSOI. Also, Fig. 4 shows the 2-D temperature distributions of the proposed structure and PSOI at $V_{DS} = 39.5$ V (the breakdown voltage of PSOI) and $V_{GS} = 4$ V. The 1-D temperature distributions of PSOI and TB-PSOI, along the AA' cut line located at 20 nm below the surface of the drift region (see Fig. 1), are presented in Fig. 5. Both these figures reveal that the self-heating effect in the proposed structure is less than that of PSOI which may be attributed to the gradual increase in the thickness of the buried-oxide layer.

Fig. 6a shows the electric field distributions for the TB-PSOI, stepped PSOI, and PSOI structures along the AA' cut line. For the PSOI structure, we assume a rectangular buried-oxide layer with a thickness of half of the buried-oxide thickness of TB-PSOI at the drain. Similar to the other two devices, the PSOI structure has a silicon window below the source region and a two-part drift region. Note that the applied voltage between the drain and source of each structure is equal to its breakdown voltages. At the breakdown voltage, the TB-PSOI and stepped PSOI structures have about the same electric field distributions with an additional peak compared to that of the PSOI device. The three peaks in the electric field distribution of the TB-PSOI and stepped PSOI structures are approximately equal which leads to a uniform electric field distribution and larger breakdown voltage. On the other hand, for the

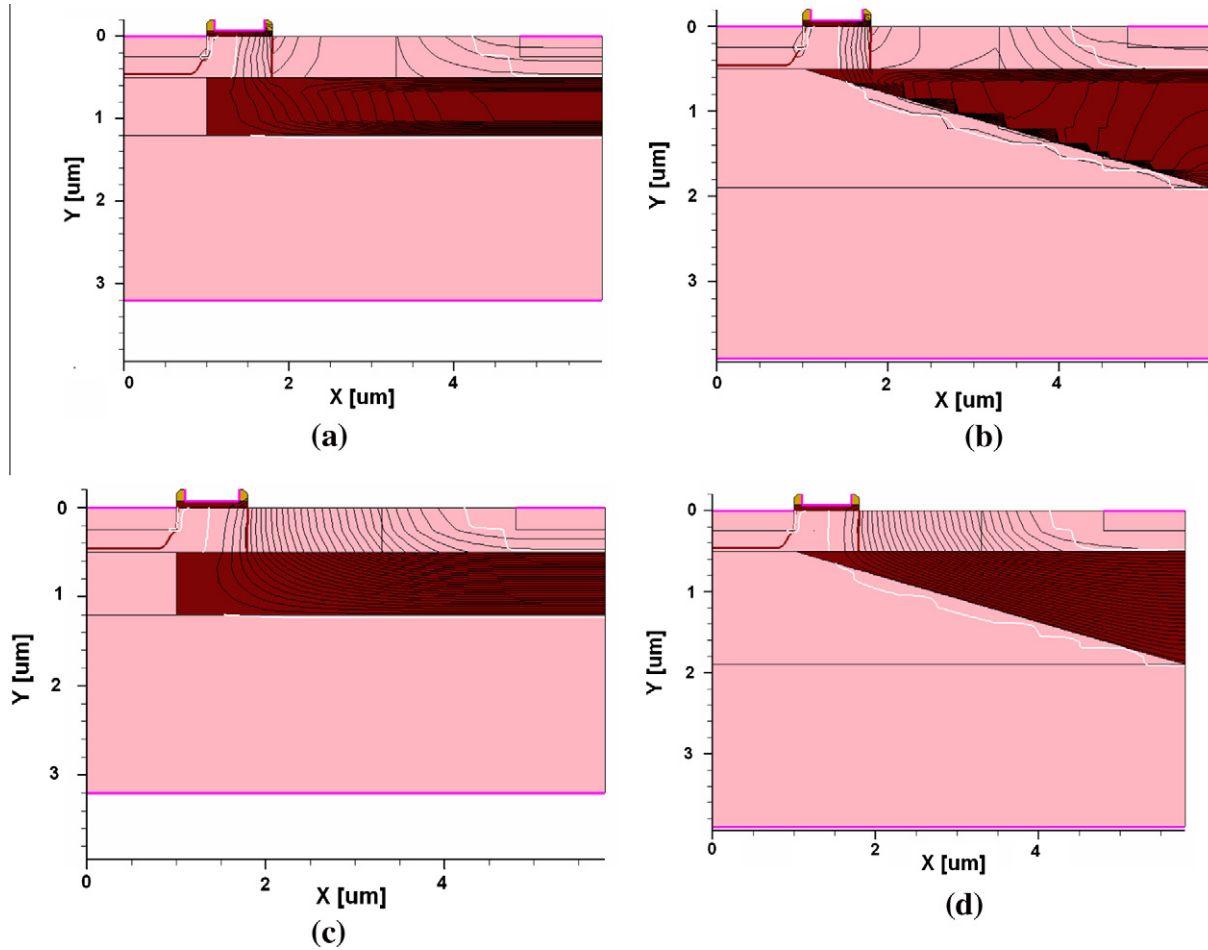


Fig. 3. The distributions for the electric fields for (a) PSOI (b) TB-PSOI, and electrostatic potentials for (c) PSOI and (d) TB-PSOI ($V_{DS} = 39.5$ V).

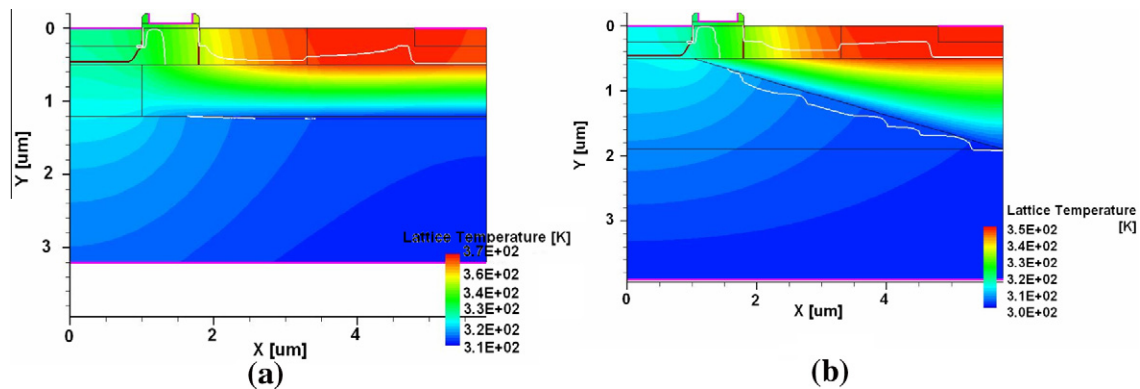


Fig. 4. The temperature distributions for (a) PSOI and (b) TB-PSOI ($V_{DS} = 39.5$ V and $V_{GS} = 4.0$ V).

case of PSOI, the heights of the two peaks are different leading to a non-uniform electric field distribution. The non-uniform electric field lowers the breakdown voltage of the PSOI structure compared to the other two devices while the drain currents of the three structures are approximately equal.

Fig. 6b shows the electric field distributions along the BB' cut line located at 100 nm above the buried-oxide layer (see Fig. 1). Since the silicon layer is relatively thin (0.5 μm) in LDMOSFETs, the electric field curves in Fig. 6a and b are similar. The potential along the HH' cut line located at 0.4 μm from the left edge of the drain region (see Fig. 1) is shown in Fig. 7. As can be seen from

the figure, the slope for the TB-PSOI and stepped PSOI structures (slope = electric field) is less than that of the PSOI structure when the same voltage is applied at the drain terminal. Therefore, TB-PSOI and stepped PSOI structures can support higher breakdown voltages. From a different perspective, the gradual increase in the buried-oxide thickness close to the drain terminal modulates the surface electric field to a more uniform distribution yielding higher breakdown voltages. It should also be noted that the close proximity of the electric field profiles for stepped PSOI and TB-PSOI structures seen in Figs. 6a and b, and 7 verifies the assumption that the stepped PSOI is a very good practical realization of TB-PSOI.

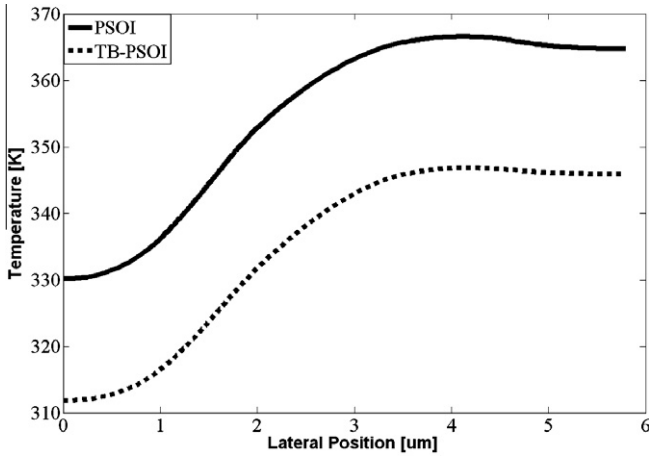


Fig. 5. The temperature (K) for the PSOI and TB-PSOI along the AA' cut line ($V_{DS} = 39.5$ V (the breakdown voltage of PSOI) and $V_{GS} = 4.0$ V).

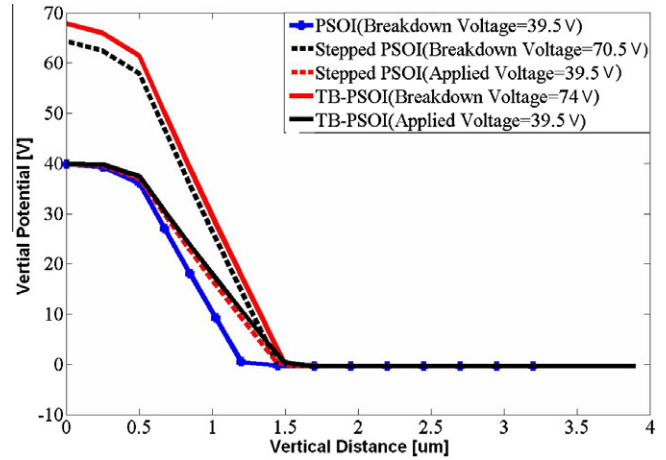


Fig. 7. Potential distributions along the HH' cut line at $0.4 \mu\text{m}$ from the edge of the drain region (see Fig. 1) for TB-PSOI, stepped PSOI and PSOI structures.

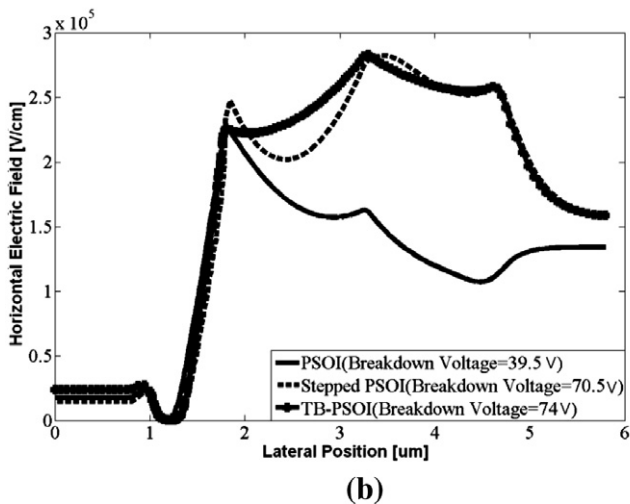
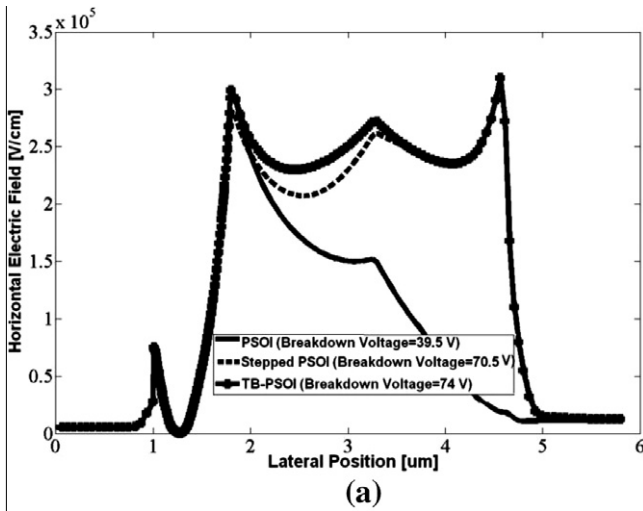


Fig. 6. Horizontal electric field profiles for TB-PSOI, stepped PSOI and PSOI structures along the (a) AA' and (b) BB' cut lines. The applied voltage between the drain and source of each structure is equal to their breakdown voltages, as shown in the figure.

4.2. Design considerations of TB-PSOI

In this part, we compare the effect of different design parameters on the breakdown voltage of the TB-PSOI, stepped PSOI, and

PSOI structures. The electric field in the drift region depends on several parameters, including the silicon-film thickness, buried-oxide thickness, drift length, buried-oxide length, and doping concentrations of the drift region. Since the simulation results of TB-PSOI and stepped PSOI structures are similar, except for the breakdown voltage dependency on the buried-oxide length and thickness, we only compare parameter optimizations for the TB-PSOI and PSOI devices.

The thickness of silicon-film in SOI technology has been reduced by scaling, which bears several benefits, including the elimination of the kink effect, enhancement of the carrier mobility, suppression of punch-through and drain-current overshoots [3]. Fig. 8 shows the breakdown voltage versus the silicon-film layer thickness for the TB-PSOI and PSOI structures assuming other design parameters are fixed as shown in Table 1. As may be seen from the figure, the maximum breakdown voltage for the TB-PSOI (PSOI) structure occurs when the thickness of silicon layer is $0.5 \mu\text{m}$ ($0.4 \mu\text{m}$). The thicknesses for the maximum breakdown voltage are not much different for the two devices. On the other hand, for any given thickness, the breakdown voltage of the TB-PSOI structure is always greater than that of the PSOI structure.

Next, the dependence of the breakdown voltage on the buried-oxide layer thickness is studied as shown in Fig. 9. As mentioned

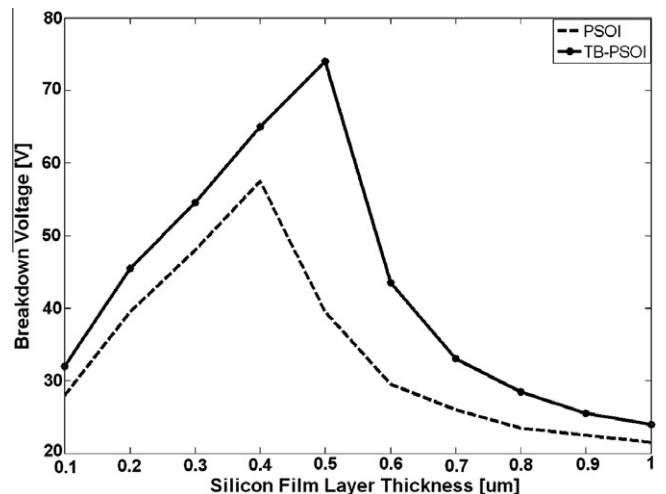


Fig. 8. Breakdown voltage as a function of the thickness of the silicon-layer for TB-PSOI and PSOI structures.

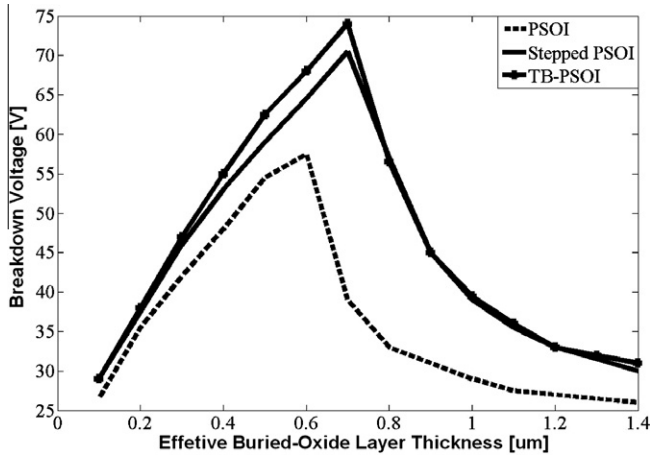


Fig. 9. Breakdown voltage as a function of the effective thickness of buried-oxide layer for TB-PSOI, stepped PSOI and PSOI structures.

before, for the comparison purpose, the same total volumes for the buried-oxide layers in three structures are assumed. Consequently, the thickness of the buried-oxide at the right end of the drain in the TB-PSOI and stepped PSOI structures is two times larger than the *effective* buried-oxide layer thickness of these structures. As the results in Fig. 9 reveal, for all thicknesses, the breakdown voltages of the TB-PSOI and stepped PSOI structures are greater than that of PSOI structure. Generally, the increase in the breakdown voltage originates from the fact that thicker buried-oxide layers could tolerate greater voltage drops [3]. Increasing the buried-oxide thickness too much, however, causes the enhancement of the peak height at the gate edge causing a lateral breakdown [3]. As shown in Fig. 9, if we increase the buried-oxide thickness further, because of lateral breakdown due to the enhancement of peak height at the gate edge, the breakdown voltage decreases. In addition, the thicknesses for the maximum breakdown voltages are similar. The results of this figure again reveal that the performance of the stepped PSOI structure is very similar to that of the TB-PSOI device. Figs. 8 and 9 indicate that the maximum breakdown voltage of the TB-PSOI structure occurs at larger silicon-film layer and effective buried-oxide layer thicknesses when compared to the case of PSOI.

Next, Fig. 10 shows the breakdown voltages of TB-PSOI and PSOI structures versus the drift length (LDD1 + LDD2). For this simulation equal lengths for LDD1 and LDD2 are assumed. For the drift

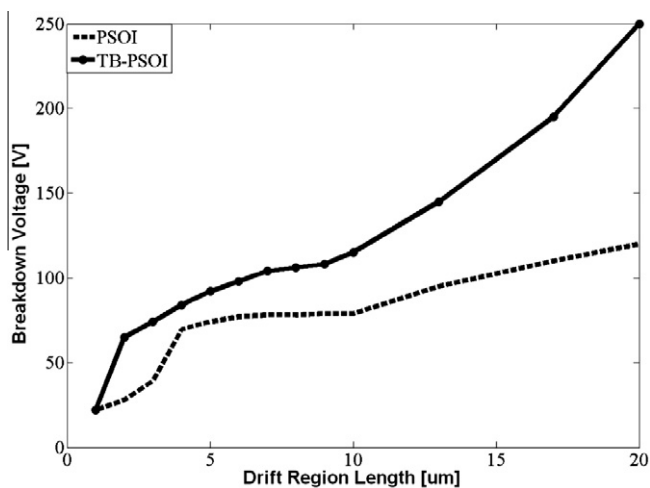


Fig. 10. Breakdown voltages versus drift length for TB-PSOI and PSOI.

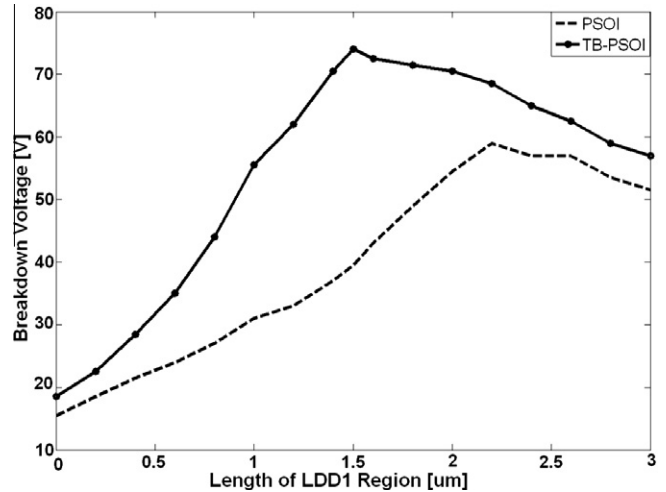


Fig. 11. Breakdown voltage as a function of the LDD1 length when the drift length is 3 μm for both TB-PSOI and PSOI structures.

length of 1 μm, the breakdown voltages of the two structures are about the same. As the drift length increases, the breakdown voltage of the TB-PSOI structure is always larger than that of the PSOI structure. Another interesting observation is that the breakdown voltage of the PSOI structure does not significantly improve beyond drift lengths larger than 4 μm. By contrast, the TB-PSOI structure achieves extremely high breakdown voltages for large drift lengths. By increasing the drift region length to 20 μm, the breakdown voltages of TB-PSOI and PSOI reach 250 V and 120 V, respectively. At this length (20 μm) the breakdown voltage of three-stepped PSOI is also very high (235 V). Note that an increase in the drift length is accompanied by lower cut-off frequency of the transistor. The results show that the maximum breakdown voltage of the TB-PSOI structure is obtained at larger drift lengths compared to that of the PSOI.

The breakdown voltage versus the LDD1 length when the drift length is fixed at 3 μm is plotted in Fig. 11. Note that the doping concentration of LDD1 is smaller than that of LDD2. Again, higher breakdown voltages are achieved for the TB-PSOI structure. The maximum breakdown voltage of TB-PSOI occurs at an LDD1 length which is a half of the drift region while the maximum breakdown

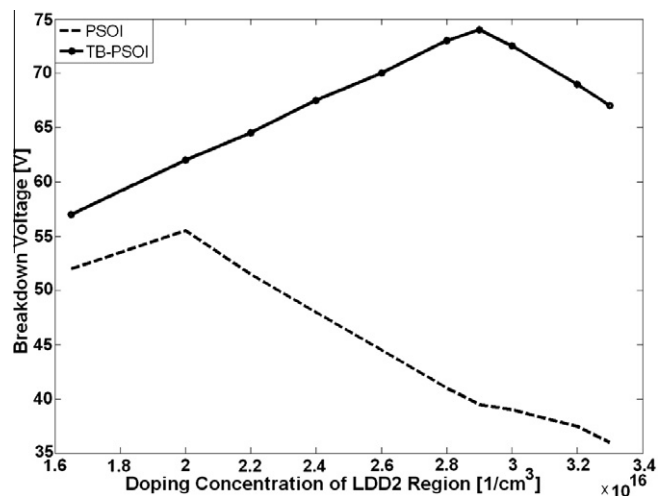


Fig. 12. Breakdown voltage versus doping concentration of LDD2 at fixed doping concentration of LDD1 ($1.65 \times 10^{16} \text{ cm}^{-3}$) for both TB-PSOI, and PSOI structures.

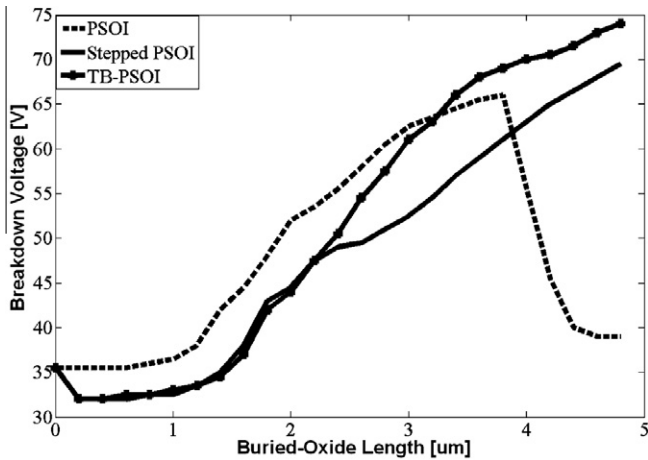


Fig. 13. Breakdown voltage as a function of the buried-oxide layer length for both TB-PSOI, stepped PSOI and PSOI structures.

voltage of PSOI is obtained at a larger LDD1 length (almost 0.75 of the total drift length).

In Fig. 12, the breakdown voltage versus the LDD2 doping concentration (N_{LDD2}) is plotted assuming a fixed doping concentration of N_{LDD1} of $1.65 \times 10^{16} \text{ cm}^{-3}$ for both structures. As the results reveal, the maximum breakdown voltage of the TB-PSOI structure occurs at a larger N_{LDD2} compared to that of the PSOI structure. Moreover, for the whole range of N_{LDD2} , the breakdown voltages of the TB-PSOI structure is greater than that of the PSOI device. The results reveal that the maximum breakdown voltage of TB-PSOI requires a higher doping concentration in the whole drift region, compared to PSOI. For a fixed total LDD length, this may be realized either by a shorter LDD1 length (Fig. 11) or a higher LDD2 doping concentration (Fig. 12).

For the results presented up to this point, it is assumed that the buried-oxide extends from the right end of source to the right end of the drain terminal. In Fig. 13, the dependence of the breakdown voltage on the buried-oxide length is shown. Note that for this study, the drain current drastically changes with the length of the buried-oxide layer. For the buried-oxide lengths smaller than $2.5 \mu\text{m}$ (smaller than half of the drift region), the breakdown voltages of TB-PSOI and stepped PSOI structures are matched well. For the lengths between $2.5 \mu\text{m}$ and $4 \mu\text{m}$ (from the middle of the drift region to its end), the breakdown voltage of the stepped PSOI is smaller than that of TB-PSOI. For the buried-oxide lengths larger than $4 \mu\text{m}$, the difference becomes insignificant. In the case of the PSOI structure, the breakdown voltages increase up to the length of $4 \mu\text{m}$ (the end of drift region). For larger lengths, where the PSOI structure becomes a conventional SOI structure, the drain current increases and the breakdown voltage suddenly drops. It should be mentioned that for the proposed structure, the breakdown voltage is proportional to the buried-oxide layer length for the lengths considered here. Also, the maximum buried-oxide layer length also corresponds to the maximum drain current due to the fact that the device becomes more similar to a full SOI structure.

Table 2

Comparison performance between the TB-PSOI, stepped PSOI and PSOI.

LDMOSFET	Breakdown voltage (V)	Drain current (μA)	Specific on-resistance ($\Omega \text{ cm}^2$)	FOM = $BV^2/R_{on,sp}$
PSOI	39.5	31.3	$3.41\text{E}-4$	4.57E6
TB-PSOI	74	30.98	$3.45\text{E}-4$	15.87E6
Stepped PSOI	70.5	30.4	$3.53\text{E}-4$	14.09E6

Finally, the impact of the proposed device on the on-resistance and current are considered. In Table 2, we present the specific on-resistance ($R_{on,sp}$) and drain current of the devices measured at $V_{GS} = 15 \text{ V}$ and $V_{DS} = 1 \text{ V}$ for the device parameters given in Table 1. These figures show that the proposed device structure does not considerably increase the specific on-resistance or decrease the drain current while significantly improves the breakdown voltage. In Table 2, also the results for a figure of merit (FOM) which is defined as $BV^2/R_{on,sp}$ (BV = breakdown voltage) are presented [33]. The values for the FOM of TB-PSOI and stepped PSOI structures are much higher than that for the PSOI device due to much larger breakdown voltage.

5. Conclusion

In this work, a novel device structure for increasing the breakdown voltage of power LDMOSFETs is proposed. The structure is based on partial SOI (PSOI) uses a triangular buried-oxide (TB) layer. To address the self-heating problem, the oxide layers are localized under the drain side of the device with P -type layer utilized underneath the source terminal. For the practical realization of the device structure, the triangular buried-oxide layer is approximated with a three-stepped oxide layer. Using a device simulator, the breakdown voltages of the TB-PSOI and stepped-PSOI structures are compared to that of the conventional PSOI device in terms of different device physical parameters. The study reveals that in most cases the stepped PSOI and TB-PSOI structures behave similarly. It also shows that the TB-PSOI and stepped PSOI structures provide higher breakdown voltages compared to that of PSOI when the drain currents are about the same. For the range of parameters used in this study, the maximum breakdown voltages of 250 V and 235 V are obtained, respectively, for the TB-PSOI and stepped PSOI LDMOSFET while the maximum breakdown voltage of 120 V is obtained for the PSOI structure.

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