Novel Efficient Adder Circuits for Quantum-Dot Cellular Automata

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Quantum Dot Cellular Automata (QCA) as an emerging nanotechnology can be considered as a possible successor for the conventional silicon MOSFET technology, in the time to come. This paper presents novel efficient designs for QCA Full Adder and Adder circuits. The layouts of the proposed designs are simple and lead to very low complexity, small area and short latency. For verifying the functionality of the circuits, all of them are simulated exhaustively using QCADesigner tool. The proposed designs are also compared with the other classical and state-of-the-art Full Adders and Adders, which demonstrates the superiority of the proposed circuits, in terms of gate count, area and latency.

Keywords: Quantum-Dot Cellular Automata (QCA), Majority Function, Full Adder, Nanoelectronics.

1. INTRODUCTION

Current silicon CMOS technology will face many significant challenges and problems at nanoscale technology nodes, which degrade its competence for low-power and high-performance applications in the near future. These challenges and problems, such as very high leakage-power consumption, short-channel effects, large parametric variations and decreased gate control can significantly restrict the design of robust and energy-efficient systems, in the time to come.¹ Due to that, researchers and scientists are working toward new technologies such as Single Electron Transistors (SET),² Nanowire transistors,³ Carbon Nanotube Field Effect Transistors⁴ and Quantum Dot Cellular Automata (QCA)⁵ as the possible successors to the conventional silicon MOSFET technology. However, among these emerging nanotechnologies, QCA could be more of interest for implementing future energy-efficient digital systems, due to its extremely low-power and high-speed operation as well as its extremely dense structure. This promising nanotechnology not only gives a solution at nanoscale, but also offers a new method of computation and information transformation.

The fundamental building block of QCA circuits are inverter and majority gates and consequently designing efficient QCA circuits using majority and inverter gates has attracted a lot of attentions. To the present time, many QCA-based circuits and systems have been presented in the literature. However, among all of these structures, arithmetic circuits could be more of interest due to their wide use in many VLSI applications such as video and image processing, DSP architectures, processors and micro/nano electronic systems.⁶ Addition is a fundamental arithmetic operation and is the base of many other more complex arithmetic operations in most of these systems. As Full Adder cell is the fundamental element of the arithmetic unit of systems and is located on the most parts of their critical paths, its performance directly affects the performance of the whole system. This means that, increasing the performance of Adder circuit is very crucial for increasing the overall performance of the systems.⁷ Therefore, designing QCA-based Adder circuits with lower complexity, smaller area and shorter delay will be highly demanded in the time to come.

In this paper new low-complexity, dense and low-latency QCA Full Adder cells and n-bit Adder circuits are proposed, which outperform the other Adder circuits, previously presented in the literature, in terms of cell count, area and latency.

The reminder of this paper is organized as follows: Section 2 reviews the QCA technology. Section 3 includes briefly descriptions about the previous works. The proposed designs are presented in Sections 4 and 5 describes the
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Fig. 1. Basic QCA cell and binary encoding.

Fig. 2. A QCA wire.

Fig. 3. Structure of a QCA three-input majority voter.

Fig. 4. QCA inverter gates.

Fig. 5. Five-input majority gates.

3. PREVIOUS WORK

Most of the previous publications in the research domain of QCA Full Adders have utilized 3-input Majority gates.9–13 The early designs of QCA Full Adder9,10 contain five 3-input Majority gate and three inverters as illustrated in Figure 6(a). In addition, some efforts have been carried out to reduce the number Majority and electrons that can move to any quantum dot within the cell through electron tunneling.8 There are only two stable configurations of the electron pair, due to the columbic interactions. Assigning a polarization, $P$, of $-1$ and $+1$ to differentiate between these two configurations, results in a binary digital system.

A series of QCA cells performs as a wire. In a QCA wire, shown in Figure 2, the binary signal propagates from input to output due to the Columbic interactions between cells.

As Majority-not gate is a universal gate and because of the nature of QCA structure, the circuits in QCA have been designed based on Majority and inverter gates. Functionality of a three-input Majority gate is shown in Eq. (1) and its QCA implementation is demonstrated in Figure 3.

$$M(A, B, C) = A \cdot (B + C) + BC$$

(1)

Up to now, two types of QCA inverters have been also proposed,8,9 which are shown in Figure 4.

Although QCA circuits have been designed based on three-input Majority gate, recently a new QCA device has been presented in Ref. [5], which can reduce the complexity, area and latency of the complex QCA circuits. This five-input Majority gate acts based on the following equation:

$$M(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE$$

(2)

The five-input Majority gate of Ref. [5] as well as another one, presented in Ref. [15], is shown in Figure 5.
inverter gates,\textsuperscript{11-13} which have been designed based on the schematic, shown in Figure 6(b).

Although these designs are based on almost similar structures, their layouts are designed differently to reduce the area, cell count and the number of clock phases. In Ref. \textsuperscript{14} a different structure has been suggested for the QCA Full Adder by the aim of reducing the number of used gates (Fig. 7). However, it has to be implemented in three dimensions that has made the fabrication process very complicated or even impossible. Recent works have presented some state-of-the-art structures for five-input Majority gate, which take advantage of simplicity and feasibility. The layouts of the Full Adders, designed based on these structures, are demonstrated in Figure 8.

\section*{4. THE PROPOSED DESIGNS}

\subsection*{4.1. Full Adder Design}

In this paper, two new QCA Full Adders are presented, using five-input Majority gates of Refs. \textsuperscript{5, 15}. The basic design of these cells follows the schematic of Figure 7, but with optimized layouts, which lead to very small area, low cell count and short delay. The functionality of these Full Adders, shown in Figure 9, can be described by the following equations:

\begin{equation}
C_{\text{out}} = \text{Majority}(A, B, C_{\text{in}}) \quad (3)
\end{equation}

\begin{equation}
\text{Sum} = C_{\text{out}} \cdot (A + B + C_{\text{in}}) + A \cdot B \cdot C_{\text{in}} \\
= \text{Majority}(A, B, C_{\text{in}}, C_{\text{out}}, \overline{C}_{\text{out}}) \quad (4)
\end{equation}

For designing a high-speed Adder, structures of the proposed 1-bit Full Adders are organized by the aim of reducing the carry propagation delay in larger designs. According to Figure 9(a), the proposed Full Adders are composed of two separate blocks. The first block, which is a three-input Majority circuit, generates the $C_{\text{out}}$ signal and the other block, which includes five-input Majority and inverter gates, generates the $\text{Sum}$ signal. Each of these blocks is implemented in a separate layer. As a result, in the upper layer of the proposed designs, $C_{\text{out}}$ signal is produced and is transferred to the main layer with the
4.2. Carry Stream Adder (CSTA)

Based on the proposed Full Adder designs, \( n \)-bit Adder circuits can be implemented. The proposed \( n \)-bit Adders follow that of a classical ripple carry adder, but with a significant modification that leads to design optimization. The new layout design of the proposed Adders leads to delay, cell count and area optimization.

By taking advantage of the proposed Full Adders, carry generator blocks are implemented in a separate layer and therefore, carry propagates just in this layer. The main origin of delay in Adder circuits is the propagation of the carry signal through the Full Adder cells. Due to that, generating and streaming of the carry signal in a separate layer, leads to reduction of complexity, delay and cell count, in the presented Carry Stream Adder (CSTA) designs. Moreover, the Sum signals are produced in the main layer by Sum generator blocks. The layouts of the proposed 4-bit and 16-bit CSTAs are shown in Figures 11(a) and (b), respectively.

In addition, by utilizing this type of design, each three-input or five-input Majority gate can be tested in a separate layer, which leads to improvement of visibility, controllability and testability of the designs.

5. EXPERIMENTAL RESULTS AND COMPARISON

5.1. Simulation Results

The proposed QCA Full Adders and carry stream adders (CSTA) are implemented and simulated using QCADesigner tool version 2.0.3.16 The following parameters are used for a bistable approximation: cell size = 18 nm, number of samples = 50000, convergence tolerance = 0.000010, radius of effect = 65.000000 nm, relative permittivity = 12.900000, clock high = 9.800000e−022 J, clock low = 3.800000e−023 J, clock shift = 0, clock amplitude factor = 2.000000, layer separation = 11.500000, maximum iterations per sample = 100. Most of the mentioned parameters are default values in QCADesigner.

A sample of input and output signals of the novel Full Adder and 4-bit Adder circuits are shown in Figures 12 and 13, respectively. The output signal of the proposed Full Adders and 4-bit CSTAs appear after \( \frac{3}{4} \) and \( 1\frac{3}{4} \) clock delays, respectively.

5.2. Comparisons

The proposed designs are compared with the conventional and state-of-the-art designs, previously presented in the literature. Comparisons between Full Adder cells are shown in Table I. According to the results, the proposed Full Adders outperform the others in terms of area, complexity and delay.
Fig. 11. The proposed CSTA (a) 4-bit CSTA (b) 16-bit CSTA.

Fig. 12. Sample input and output signals of the proposed full adders.
Novel efficient Adder circuits for Quantum Dot Cellular Automata (QCA) Full Adder and Adder circuits have been presented in this paper. The simple and efficient layouts of the proposed structures result in a low number of gates, small area and short delay. As the main source of the delay in Adder circuits is the propagation of the carry signal through the Full Adder cells, the novel Full Adders and Carry Stream Adders (CSTA) have been designed by the aim of restricting the effect of the carry propagation delay on the delay of the Adders, to reach more high-speed operation. Exhaustive simulations using QCADesigner tool have verified the functionality of the presented structures. In addition, comparisons demonstrate the superiority of the proposed designs, compared to the conventional and state-of-the-art QCA Full Adders and Adders, in terms of area, gate count, and latency.

6. CONCLUSION

Novel efficient designs for Quantum Dot Cellular Automata (QCA) Full Adder and Adder circuits have been presented in this paper. The simple and efficient layouts of the proposed structures result in a low number of gates, small area and short delay. As the main source of the delay in Adder circuits is the propagation of the carry signal through the Full Adder cells, the novel Full Adders and Carry Stream Adders (CSTA) have been designed by the aim of restricting the effect of the carry propagation delay on the delay of the Adders, to reach more high-speed operation. Exhaustive simulations using QCADesigner tool have verified the functionality of the presented structures. In addition, comparisons demonstrate the superiority of the proposed designs, compared to the conventional and state-of-the-art QCA Full Adders and Adders, in terms of area, gate count, and latency.
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